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SIMULATION OF A NOVEL BIPOLAR-FET TYPE-S, NEGATIVE RESISTANCE CIRCUIT

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A new circuit which uses FET and bipolar transistor is given. It exhibits Type-S differential negative resistance and a theoretical explanation is appended along with PSPICE simulation.

Keywords: Negative resistance; Novel circuit; Bipolar FET device; Circuit simulation

1 INTRODUCTION

Solid state devices possessing differential negative resistance are very useful for a wide range of applications involving oscillation, amplification and logic operations.

Tunnel diodes can be used as microwave oscillator, tuned amplifier, mixer, logic gates, flip flops, counters, table multivibrator etc. Similarly, UJT can also be used as a relaxation oscillator. Wide applications of SCR in control systems are well known. However, the value of their negative resistance can be adjusted only slightly. Moreover, since they are not made of standard FET or bipolar transistors or both, their fabrication and mass production as integrated circuits is not feasible.

Another approach for inventing new solid state negative resistance devices is to combine FET and bipolar transistor with resistors. The first circuit which exhibited negative resistance characteristics and did not use internal bias was found in 1965 by Nagata [1].

After that a few more circuits were added. Basic procedure to generate these circuits was try and hit. No systematic method exists even today.

2 ALGORITHMS FOR GENERATING SUCH DEVICES

Recently in 1983, Chua, Yu and Yu [2] gave a somewhat reliable procedure to generate Type-N devices. Many circuits using this procedure are generated.

This procedure only helps in discriminating possible candidates which may exhibit negative resistance characteristics. This also cannot tell absolutely whether or not the circuit

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will exhibit the negative resistance. The procedure is based on observations. A final 'yes' can be said only after simulation using SPICE or fabricating and checking the circuit.

Kumar and Nayak [3] proposed the algorithm in 1984 for generating type-S devices. However, this algorithm is also not ultimate and one cannot be one hundred percent sure whether or not the circuit is desirable. But this method is very efficient and gives a quick estimate about resistance values. Also it is not time-consuming and tells us whether the circuit will exhibit negative resistance.

3 NOVEL TYPE-S CIRCUIT DEVELOPED

A new circuit (Fig. 1) which uses two resistors, one n-channel FET and one n-p-n Bipolar transistor is presented. This circuit gives wide flexibility in curves and the design is simple since calculations involved are not very complex.

The operation of the circuit is like this. The circuit has $V_{GS} = 0$, so the current will pass through R_1. FET and R_2 initially, I_B flowing is very small. So voltage V_{BE} will be developed at T_2. When this voltage is equal to the cut in voltage of the base emitter junction 0.6 Volts, T_2 goes in saturation and V drops giving very high I.

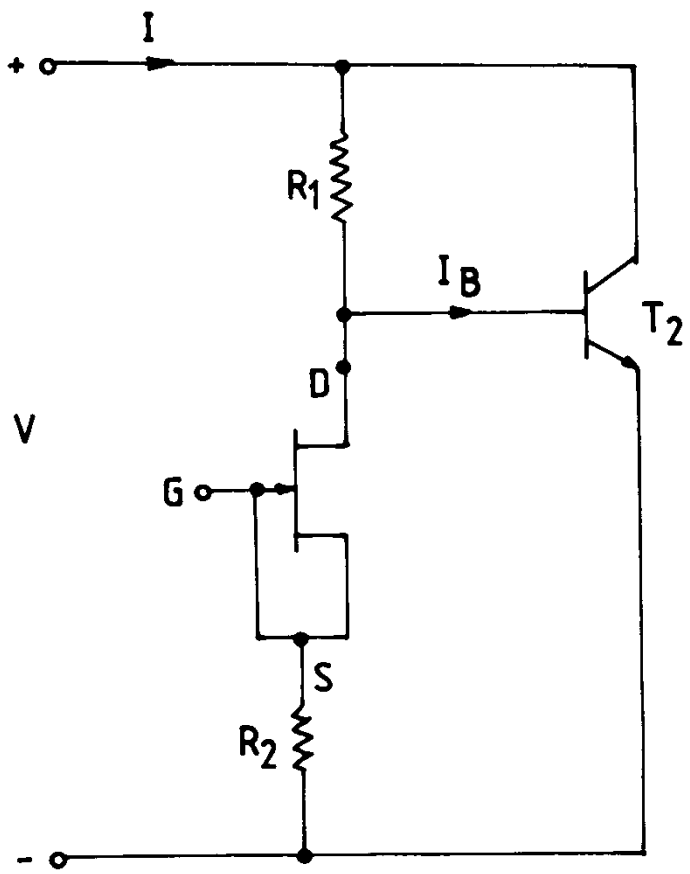

FIGURE 1

4 THEORETICAL EXPLANATION OF THE NEW CIRCUIT

The current and voltage in the new circuit are shown in Figure 1. Now,

$$V_{BE} = \frac{R_2}{R_1 + R_2} V \tag{1}$$

and

$$\frac{V - V_{BE}}{R_1} = I - \beta I_B \tag{2}$$

when $V_{BE} = 0.6$, transition occurs from Region 1 to Region 3.

The voltage at which this takes place is from equation (1):

$$V = \frac{R_1 + R_2}{R_2} \times 0.6 \tag{3}$$

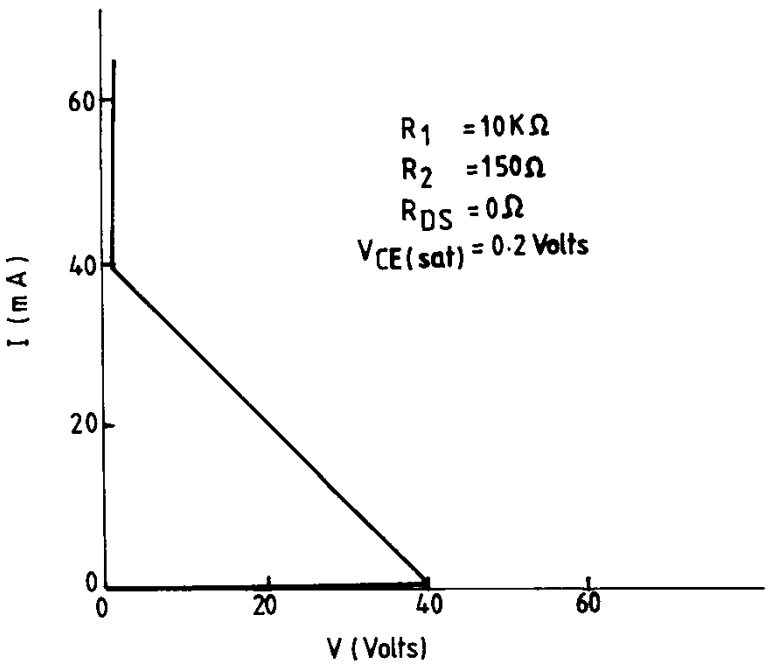

FIGURE 2

up to when the transition took place I_B was very small, not enough to put T_2 in saturation.

$$\begin{aligned} I &= \frac{V_{BE}}{R_2} + \beta\left(\frac{V - V_{BE}}{R_1} - \frac{V_{BE}}{R_2}\right) \\ &= \frac{V_{BE}}{R_2} + \beta\frac{V}{R_1} - \beta\frac{V_{BE}}{R_2} \\ &\cong \beta\left[\frac{V}{R_1} - \frac{V_{BE}}{R_2}\right] \end{aligned} \tag{4}$$

since V is very high and $R_1 > R_2$. For the values of the example

$$I = 0.2 \times 10^{-3}\,\text{amp.}$$

When transition takes place in Region-3 of Type-S curve, current of the order of 40 mA flows in the circuit with $V = V_{CE} = 0.2$ Volts which is saturation collector emitter voltage. The PSPICE simulation results are shown in Figure 2.

I flowing at this time depends on I_{GS} which is only several ohms (typically 5 ohms).

The resistance between D and S is several hundred kilo/ohms to several kilo/ohms. Hence, while finding V_{BE}, R_2 should be replaced by $R' = R_2 + r_{DS}$. We can design considering FET only without R_2 and necessary r_{DS}. While fabrication of this is useful, R_2 gives flexibility to locate transition points e.g. peak and valley points. Other FET bipolar circuits with more than two active devices are given in [4].

5 CONCLUSION

A new FET-Bipolar negative resistance Type S circuit is presented, explained and simulated. Design is simple in this case. The field is new and not much work has been done especially in FET circuits. The scope for future research is very wide.

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