Active and Passive Elec. Comp., 2002, Vol. 25, pp. 215–223

Taylor & Francis
Taylor & Francis Group

ANALYSIS AND SIMULATION OF FUNCTIONAL STRESS DEGRADATION ON VDMOS POWER TRANSISTORS

M. ZOAETER[a,*], B. BEYDOUN[a], M. HAJJAR[a], M. DEBS[a] and J-P CHARLES[b]

[a]*Laboratoire de Physique des Matériaux, Faculty of Science-I, Lebanese University, P.O.Box 13-5789, Beirut 1102-2070, Lebanon;* [b]*Matériaux Optiques, Photonique et Systèmes (MOPS), CLOES, Supelec, 2, rue Edouard Belin, 57070 Metz, France*

(Received 5 September 2001; In final form 6 November 2001)

The use of VDMOS transistor under certain functional stress conditions produces a modification of its physical and electrical properties. This paper explores the physical analysis and SPICE simulation of the degradation effects related to the component micronic structure, and points out the degraded parameters following this stress.

INTRODUCTION

The use of VDMOS transistor in the field of power electronics has increased widely due to its high input impedance, ease of isolated-grid control and negative temperature coefficient of the drain current that prevents thermal racing.

The use of power VDMOS under certain stress conditions may lead to a modification of its physical and electrical properties. There are many types of stress: stress by irradiation for which the component operation is altered following the action of the radiation on the material [1–4]; thermal stress where the temperature effect is a dominant factor in degradation; and electrical stress which can arise from the application of a power surge or intense current peaks on the component grid. In an industrial circuit, the coercive use of the component satisfying a functional need often produces degradations of complicated origins. Degradations corresponding to a functional stress in an inverter circuit are the subject of this communication. The study explores the analysis and the simulation of the degradations effect related to the component micronic structure and points out the sensitive parameters. The alteration of these parameters modifies the VDMOS operation and their value changes give a measure of their electrical properties degradation degree and identifies the degradation mechanisms.

STRESS STUDY IN VDMOS

The considered power VDMOS transistor has a vertical structure. Drain is located on the back of the plate, grid and source are on the upper surface (Fig. 1). The current flows vertically [5].

* Corresponding author.

ISSN 0882-7516 print; ISSN 1563-5031 online © 2002 Taylor & Francis Ltd
DOI: 10.1080/0882751021000012517

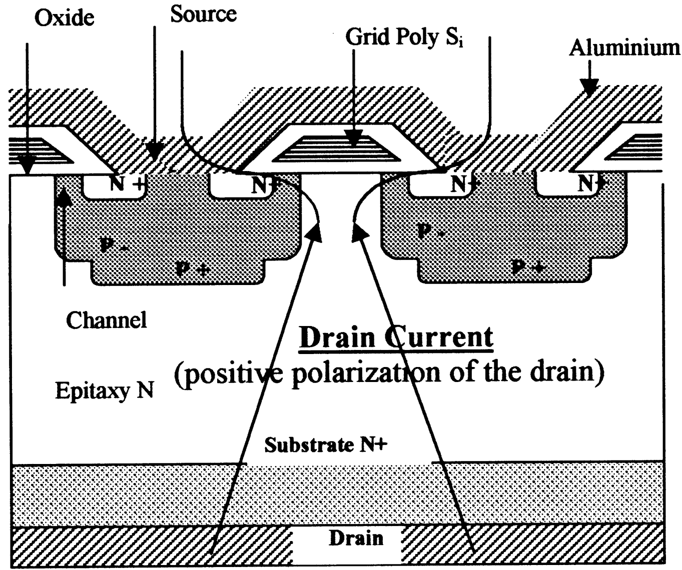

FIGURE 1 Structure of VDMOS transistor.

The thousands of cells that constitute the component behave so that their currents are in parallel. The VDMOS has two operating states: the first, called "conduction" state, is characterized by the formation of an inversion channel under the effect of positive grid–source voltage and, hence, by the flow of a drain current whose value depends on the physical and technological structure parameters, and the applied voltages; the second called "blocked" state, is characterized by a grid–source voltage smaller than a threshold value for which there is no

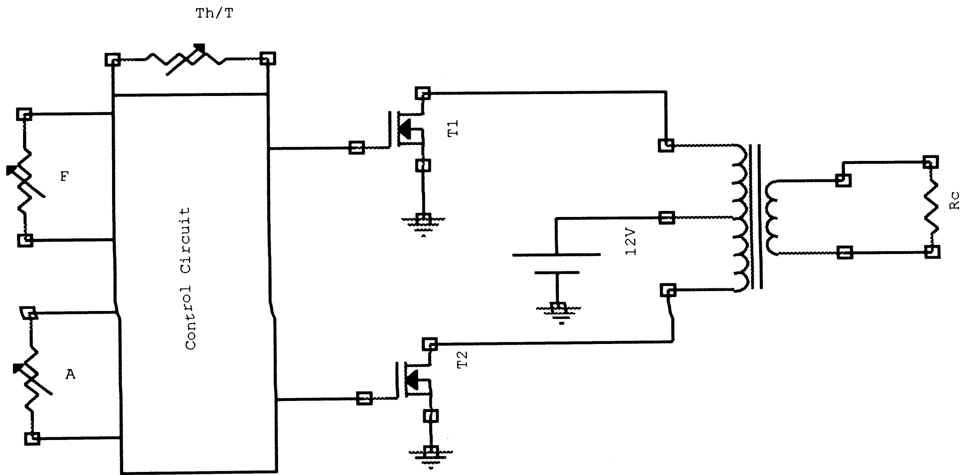

FIGURE 2 Inverter used to generate and study functional stress. Drain current is 10 A. Operating temperature is maintained below 35 °C. Transistors are HARRIS RFP70N03.

current flow; the quasi totality of the applied grid–drain voltage is then carried out by the transistor drift region.

In order to control the functional stress conditions, we have designed an experimental device to simulate the "normal" conditions of the coercive use of the VDMOS within an inverter circuit (Fig. 2). The control circuit permits variation of the frequency, of the cyclic ratio, and of the grid driving-bias.

For this study, we have used a group of VDMOS components RFP70N03 manufactured by HARRIS Inc. Our procedure involves running the VDMOS in the inverter circuit while maintaining their temperature at room temperature or close to it, below 35 °C. Stress operating conditions correspond to a 10 A drain current value with bias varying from 14 V to 24 V according to the circuit load. Initial stress duration was 4 hours. For every component of the batch under study, electrical characteristics determination is done before and after stress. Full stress analysis involves measuring the electrical properties and comparing them with those obtained from SPICE simulation.

ANALYSIS OF THE OPERATIONAL STRESS EFFECT

After subjecting the VDMOS transistor to stress, comparing the electrical properties with those obtained before the stress proves that:

$I_D = \mathrm{f}(V_{GS})$

On the characteristics curve $I_D = \mathrm{f}(V_{GS})$, we observe a shift in the transistor threshold voltage due to the applied stress (Fig. 3). In fact, the threshold voltage corresponds to a particular

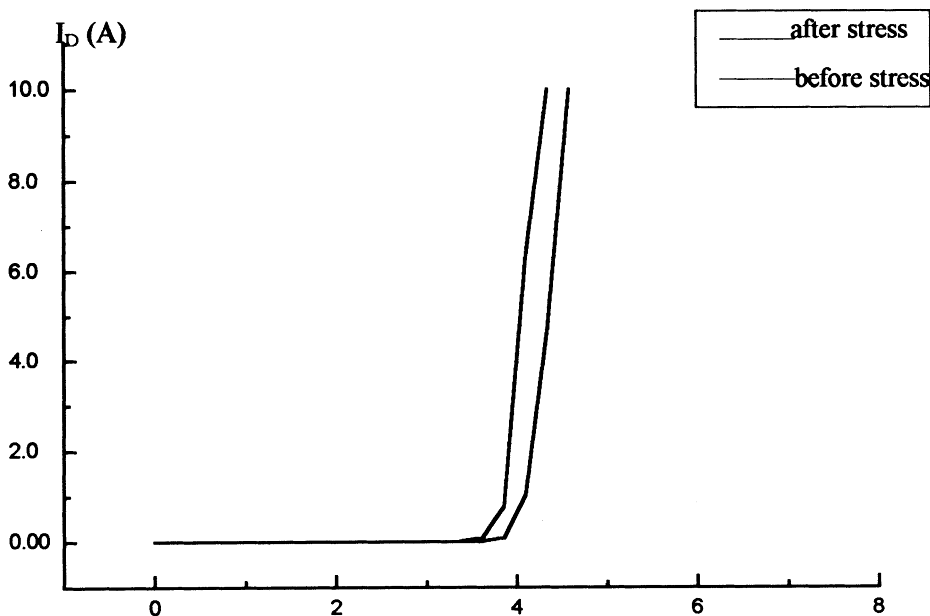

FIGURE 3 Variation of drain current versus grid voltage before and after stress.

value of the grid voltage, beyond which the transistor begins to conduct [6]. This voltage can be written in the form:

$$V_T = -\frac{Q_{ss}}{C_{ox}} + \phi_{ms} + 2\phi_F + \sqrt{2\phi_F\phi_B} \tag{1}$$

$$\phi_B = \frac{2qN_{A\max}\cdot\varepsilon_o\varepsilon_{ox}}{C_{ox}^2} \tag{2}$$

where ϕ_B is the substrate internal potential, ϕ_F is the Fermi potential given by:

$$\phi_F = U_T \mathrm{Ln}\left(\frac{N_{A\max}}{n_i}\right) \tag{3}$$

$N_{A\max}$ is the maximal value of the substrate doping (region P), and Q_{ss} represents the total interface states charge.

The trapped charge in the oxide due to electrical stress arises from the action of the hot carriers produced in the channel or at its extremities when pulses are applied on the grid. The electrons have a great mobility in the oxide and do not remain trapped. Only positive charge persists in the oxide due to their low mobility. In the actual experimental conditions, the produced charge levels are shallow and they are considered here as interface states. Their presence affects the conduction in the channel. Because of the increase in the threshold voltage (Fig. 3) we deduce that the interface charge produced by this functional stress is negative. These interface states are related to acceptor levels located in the first third of the forbidden band, taken from the valence band [7].

$I_D = \mathrm{f}(V_{DS})$

Due to electric stress, we observe that the saturation current for a given grid voltage (Fig. 4) undergoes a considerable drop. The explanation of this drop lies in the modulation phenomenon of the carrier mobility in the inversion layer. In fact, the mobility in the channel is a function [8] of the substrate doping, the electric field, the silicium crystalline orientation, the substrate potential, the temperature, and the fixed charge in the oxide. Many studies have shown the electron local variations in the inversion layer [9–11]. A simplified expression of the carrier mobility in the channel has been established [12]:

$$\mu_{\text{eff}} = \frac{\mu_0}{[1+(|E_x|/|E_c|)][1+(|E_y|/|E_0|)]} = \frac{\mu_0}{[1+(V'_{GS}-\phi_s)/(T_{ox}\cdot E_c)][1+(\mathrm{d}\phi_s/(\mathrm{d}y\cdot E_o))]} \tag{4}$$

with

$$V'_{GS} = V_{GS} + V_{FB}$$

where

$$V_{FB} = \frac{Q_{ss}}{C_{ox}} - \phi_{ms}$$

μ_o is the weak field mobility, E_x and E_y represent the transversal and longitudinal components of the electric field respectively, E_o is the amount of the longitudinal critical field, beyond it the electron velocity becomes saturated, E_c is the transverse electric field, V'_{GS} is the rms voltage applied to the grid, V_{FB} is the flat-band voltage, ϕ_s is the electrostatic potential on the semiconductor surface, y is the coordinate along the longitudinal source-drain direction, ϕ_{ss} is the total charge in the thin grid oxide and at the Si–SiO_2 interface, T_{ox} is the thickness of the grid

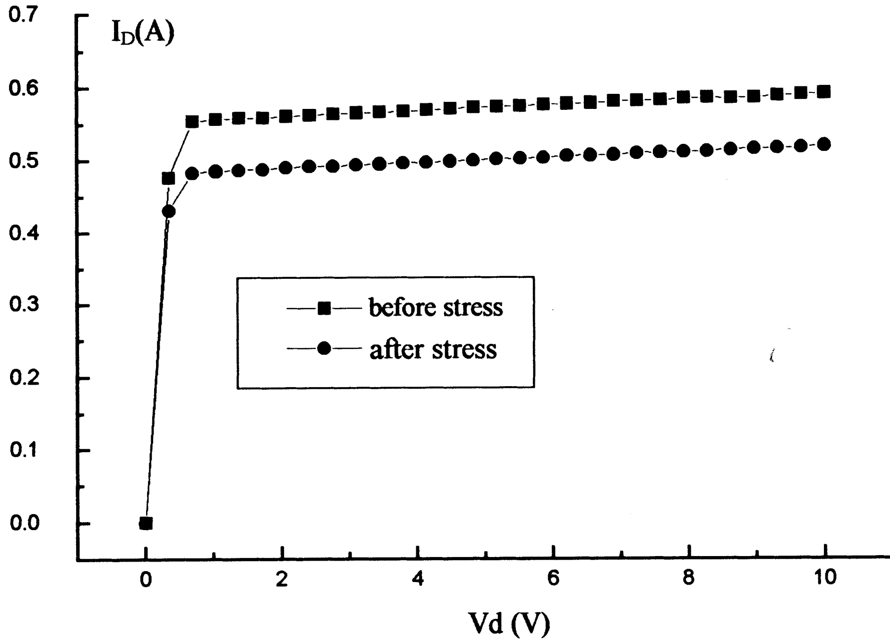

FIGURE 4 Drain current characteristics before and after stress for $V_G = 3.8$ V.

oxide, $C_{\mathrm{ox}} = \varepsilon_o \varepsilon_{\mathrm{ox}}/T_{\mathrm{ox}}$ is the thin oxide capacitance per unit area, and ϕ_{ms} is the difference in the extraction works between the metal of the grid electrode and the semiconductor.

The saturation of the carrier velocity in the channel is intrinsically taken into consideration in this relationship when the field $\mathrm{d}\phi_s/\mathrm{d}y$ becomes much greater than the critical field E_o.

For a given grid voltage, the value of the saturation velocity determines the level of the saturation current.

The electrical stress introduces charges to the Si–SiO_2 interface whose effect is to increase the probability of collisions between the inversed layer carriers and the fixed ones. The carrier velocity decreases resulting in a reduction of the carrier mobility value. Consequently, a drop in the saturation current is observed.

In order to complete our analysis, we put many components under stress for a long period of time (multiple 24 hours operation times). The characterization that followed these experiments did not give any additional information to those obtained from the initial tests *i.e.* the degraded parameters reach a steady state value as no further variation is observed. Consequently the stress duration seems to have no direct effect on the functional stress phenomenon.

VDMOS MODEL AND SIMULATION OF THE PHENOMENON

In order to confirm our analysis, we performed SPICE simulations of the VDMOS before and after the stress. For this purpose, many models for the power VDMOS transistor, compatible with the SPICE software, have been suggested recently [13–16]. We use a model [17] which describes the active part (inversion channel) of the transistor by the SPICEMOS transistor model adding other elements to this software (Fig. 5) in order to have a macro model able to interpret the electrical behavior of the device (Fig. 6).

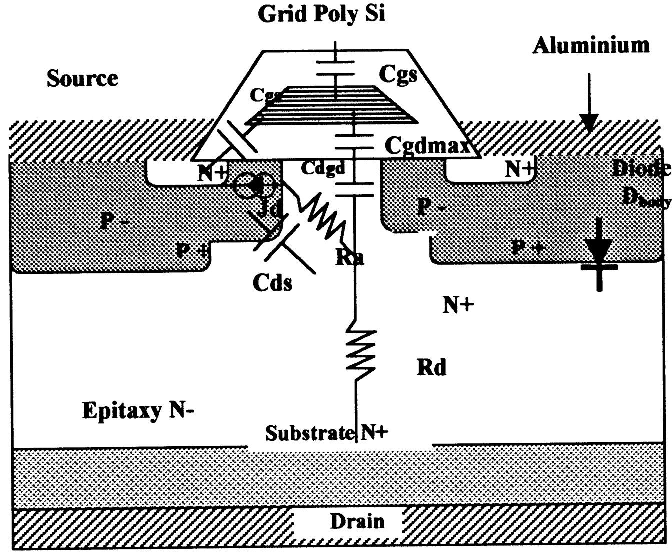

FIGURE 5 Cross section of VDMOS cell showing steady and transient elements included in the simulation model.

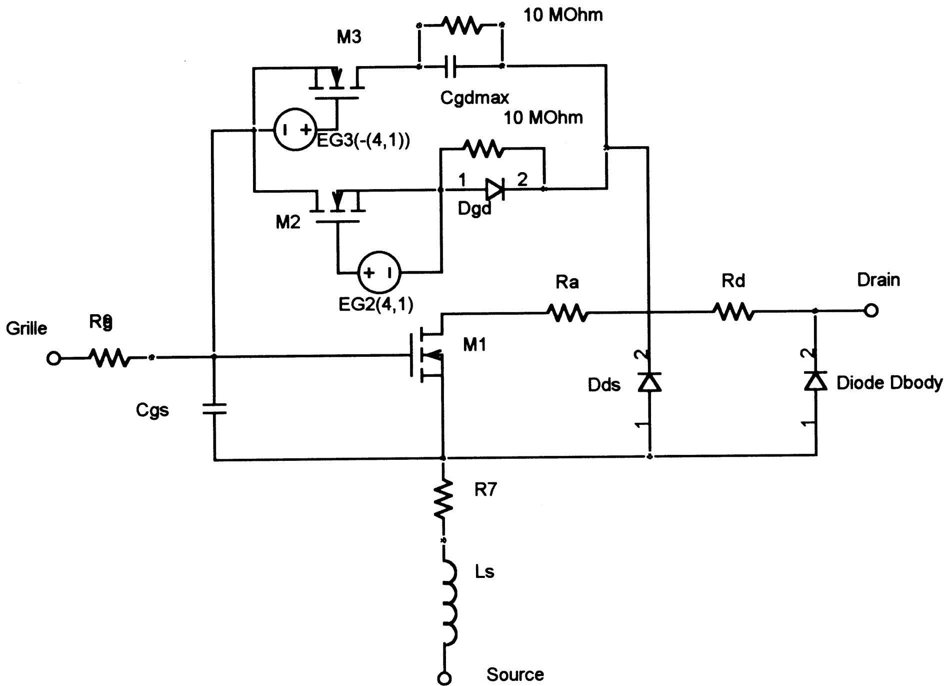

FIGURE 6 SPICE macro model of VDMOS transistor.

Based on the physical and electrical analysis of the VDMOS structure, the steady operation is obtained by representing the conduction channel by a MOS transistor (MI) acting only by its current generator J_d to which an access resistor R_a and a drift region resistor R_d are added externally in series with the drain electrode. The level 3 of SPICE MOS transistor model is

taken for this MOS MI. This level is selected because its expression for the active carriers mobility is similar to that established for the drain current of a VDMOS transistor.

In dynamic operation, the inter-electrode capacitors C_{gs}, C_{gd} and C_{ds} are taken into consideration. The grid-source capacitor C_{gs} is considered, as a first approximation, independent of the bias voltage; the drain-source capacitor C_{ds} is a real diode transition capacitor and is modeled by a SPICE diode D_{DS}; the grid-drain capacitor C_{gd} is modeled by an oxide capacitor C_{gdmax} in parallel with a diode D_{GD}. Another diode D_{body} is added to take into account the reverse conduction and the charge-storing effect during its overlay setting. The configuration is completed by noise elements (the grid polysilicium resistor R_g, the resistor R_g, and the source inductor L_s).

Model parameters are obtained by this characterization process before and after stress. The same experimental conditions have been reproduced for the SPICE simulation.

RESULTS OF SPICE SIMULATION

$I_D(V_{DS})$

As seen above, the carrier velocity determines the level of saturation current. SPICE takes this effect into consideration [18] through the carrier limit velocity V_{max}. Its value is determined case by case depending on the device, and by comparing the results obtained by simulation to those obtained from experiment (for the static saturated characteristics). It appears here that the value $V_{max} = 4950\,\mathrm{cm}^2/(\mathrm{V} \cdot \mathrm{s})$ before stress is reduced after stress to $4100\,\mathrm{cm}^2/(\mathrm{V} \cdot \mathrm{s})$ (Fig. 7). This does confirm the analysis performed on experiment which relates the degradation characteristics to the problem of the mobility modulation inside the channel.

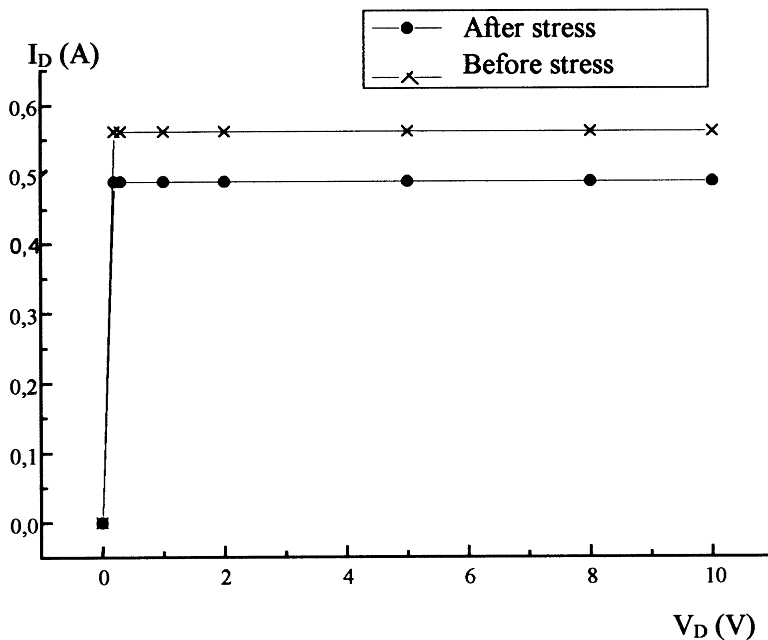

FIGURE 7 Simulation of the drain current characteristics before and after stress for $V_G = 3.8$ V.

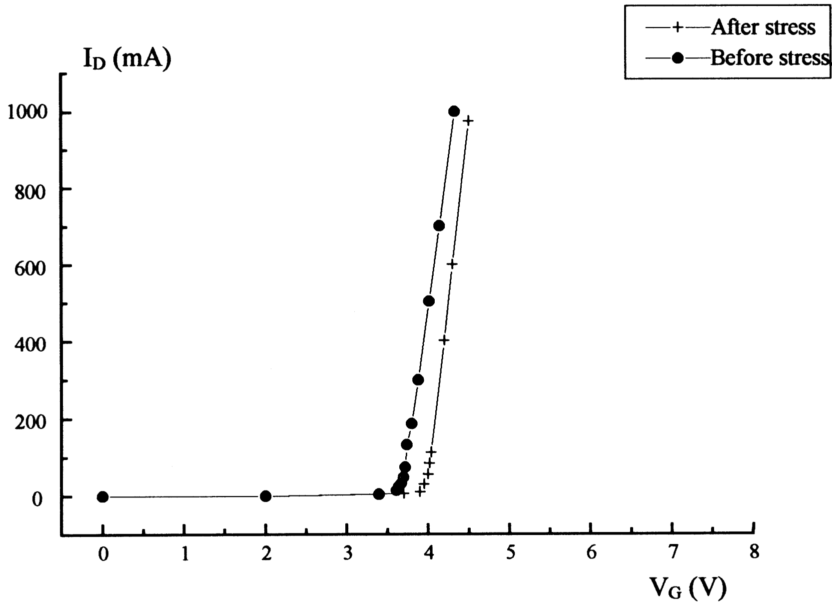

FIGURE 8 Simulation of the drain current versus grid voltage characteristics: before and after the functional stress.

$I_D(V_{DS})$

The fact that the fixed charge at the interface in SPICE simulation is taken into consideration confirms the analysis of the threshold voltage shift. In fact, we obtain the same shift in the threshold voltage before and after the stress (Fig. 8) as the experimentally determined value.

CONCLUSION

In this paper, we have studied the functional stress effect in VDMOS power transistors operating in an inverter circuit. Analysis of this effect related to the degradation of the electrical transistor characteristics of the transistor has been presented. The analysis and the simulation provide an explanation to this effect through the modification of the density of the trapped charge at the Si–SiO_2 interface. The applied functional stress results in the creation of shallow negative charge that can be considered as interface states. Their presence affects the conduction phenomenon in the channel. The density variation of the trapped charge produces a shift in the threshold voltage and causes degradation of the carrier mobility in the component channel, and thus leading to a reduction in saturation current.

References

[1] Buchanan, B. L., Neamen, D. A. and Sheld, W. M. (1978). SOS device radiation effects and hardening. *IEEE Transaction on Electron Devices*, **25**(8), 959–970.

[2] Azais, B., *et al.* Neutron induced damage in linear integrated circuits: Ionizing effects contribution. *IEEE 4th European Conference on Radiation and its Effects on Components and Systems Proceedings 1997.* Cannes, 15–19 September.

[3] Ma, T. P. and Dressendorfer, P. V. (1989). *Ionizing Radiations Effects in M.O.S Devices and Circuits.* John Wiley, New York.
[4] Yih, C.-M., Cheng, S.-M. and Chung, S. S. (1998). A new approach to simulating n-MOSFET gate current degradation by including hot-electron induced oxide damage. *IEEE Transaction on Electron Devices*, **45**(11), 2343–2348.
[5] Baliga, B. J. (1995). *Power Semiconductor Devices.* PWS Publishing Company.
[6] Grove, A. S. (1967). *Physics and Technology of Semiconductor Devices.* Edition J. Wiley and Son.
[7] Mathieu, H. *Physique des Semi-Conducteurs et des Composants Electroniques.* éditeur Masson.
[8] Mena, J. G. (1981). High frequency performance of VDMOS power transistors. *M. A. Sc. Thesis.* University of Toronto, Canada.
[9] Rish, L. (1983). Electron mobility in short- channel MOSFET's. *IEEE Transaction on Electron Devices*, **ED-0**(8), 1168–1171.
[10] Sun, S. C. and Plummer, J. D. (1980). Electron mobility in inversion and accumulation layers on thermally oxidized silicon surfaces. *IEEE Transaction on Electron Devices*, **ED-27**, 671–683.
[11] Fung, F. F. and Fowler, A. B. (1970). Hot electron effect and saturation velocities in silicon inversion layers. *J.A.P*, **14**, 1825–1831.
[12] Vassilieff, G. (1971). Modèle du transistor MOS. Influence de variation de la mobilité des porteurs. *Thèse.* Université Paul Sabatier, Toulouse.
[13] Dolny, G. M., Ronan, H. R. and Wheatley, C. F. A SPICE II subcircuit representation for power MOSFET-s using empirical method. *The Power Electronics Design Conference Proceedings 1985*. October, pp.'147–153.
[14] Hancock, J. M. (1988). Enhanced techniques for SPICE modelling of power MOSFET's. *PCI proceedings*, June 1988.
[15] Castro Simas, M. I., Piedade, M. S. and Costa Freire, J. (1989). Experimental characterization of power VDMOS transistors in commutation and a derived model for computer aided design. *IEEE Transaction in Power Electronics*, **4**(3).
[16] Xu, C. H. and Schroder, D. Modelling and simulation of power mosfets and power diodes. *IEEE PESC'88 RECORD.* Kyoto, April, pp. 76–83.
[17] Cordonnier, C. E., Maimouni, R., Tranduc, H., Rossel, P., Allain, D. and Napieralska, M. (1989). *SPICE Model for TMOS Power MOSFET's Application*, Note Motorola Semi conductor, AN 1043.
[18] Antognetti, P. and Massobrio, G. (1988). *Semiconductor Device Modelling with SPICE*, Edition Mc Graw-Hill Book Company.