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Properties of MOS Capacitors Produced on SiGe Formed by Ge-implanted Si

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Abstract

Metal-oxide-semiconductor (MOS) capacitors fabricated on Ge-implanted Si have been investigated by using C-V and G-V measurements. The control sample on pure Si substrate yielded normal C-V and G-V characteristics. The Ge-implanted MOS samples exhibited anomalous C-V and G-V behavior. The C-V curves of the samples were strongly frequency dependent both in the accumulation and inversion regions. They shift almost in parallel to higher values with decreasing frequency, reaching the oxide capacitance value in the quasi-static (QS) measurement. A band structure and equivalent circuit model were introduced to explain this and other features of the experimental observations. It is shown that the presence of a thin SiGe layer and/or trap states related to this layer may cause a frequency dispersion in the accumulation region of the C-V curves of MOS capacitors.

1. Introduction

In recent years, various applications of SiGe/Si heterostructures have been reported. It is well established that high-quality heterojunctions can be produced by using Si and SiGe alloys to engineer the band gap for optoelectronic and bipolar devices [1]. The bandgap engineering of the commensurately grown Ge_xSi_{1-x} on Si offers the possibility of fabricating heterojunction bipolar transistors, modulation-doped field-effect devices, long-wavelength optoelectronic devices, and tunneling and superlattice devices [2-4]. $Si_{1-x}G_{ex}$ layers on Si substrate have been grown by various techniques, which include molecular beam epitaxy (MBE), chemical vapor deposition (CVD), and their various versions. Ge implantation followed by a solid phase epitaxy (SPE) into Si has also been investigated as an alternative technique for the $Si_{1-x}G_{ex}$ growth [5,6]. It has been shown that $Si_{1-x}G_{ex}$ layers can be formed successfully by Ge implantation [5,6]. Ge implantation has also been used for other applications, such as preamorphization in shallow $p^+ - n$ junction

production [7,8] and reduction of dopant diffusion in CMOS fabrication [9]. If SiGe is to be used in the above-mentioned applications, a high quality dielectric layer such as SiO_2 should be formed on it. Thermal oxidation of SiGe has been extensively studied because of its superiority in the production of MOS devices. It was found that Ge atoms are segregated out from the growing SiO_2 in the case of high temperature atmospheric pressure oxidation of SiGe [10-15]. Segregated Ge atoms pile up at the interface and form an epitaxial Ge-rich layer between SiO_2 and the underlying Si substrate. In recent years several attempts to avoid the Ge pile up problem have been reported [16-18]. Low temperature oxidation [16], plasma-assisted oxidation [17], Electron Cyclotron Resonance (ESC) oxidation [18] are among these studies recently reported.

Electrical properties of the interface between SiO_2 and the substrate are crucially important in devices which use SiO_2 as an insulating or passivating layer. The Ge-pile up and the formation of a Ge-rich layer at the interface are expected to modify the electronic structure considerably. In spite of a large number of reports on the oxidation kinetics and structural properties, only a few studies have been reported on the electronic structure of the interface [16,19,20]. In these studies only the density of states was estimated and no details of the electronic structure were given. Moreover, the formation of an epitaxial SiGe layer below SiO_2 introduces an asymmetric band structure due to presence of a SiGe/Si heterojunction which is known to have large band edge discontinuity in the valence band compared to that in the conduction band. This should lead to differences in p- and n-type samples. Such a difference was indeed shown to exist in a previous study [20]. It is of both scientific and technological interest to elaborate this observation. Investigations published so far on the electrical properties have mostly dealt with n-type substrates. A few C-V results on p-type samples were either for very thin SiO_2 layer without Ge-pile up [19] or without detailed analysis [20].

In this work we report on electrical properties of MOS structures fabricated on Ge-implanted p-type Si using C-V and G-V measurements. The effect of SiGe formation at the interface due to Ge pile up is expected to be significant in these sample types because of the valence band discontinuity. A Si control sample was also fabricated for comparison. It was found that MOS characteristics of Ge-implanted samples were different than that of control sample. The observed difference can be described by the properties of the band structure formed at the interface. A model incorporating a SiGe/Si heterojunction was shown to be consistent with the observation.

2. Experimental Details

The samples used in this work were p-type <100> Si with resistivity of 25-30 Ω-cm. They were implanted with 40 keV ^{74}Ge ions to the doses of $1x10^{15}$ cm^{-2} and $1x10^{16}$ cm^{-2}. A pure Si control sample was also produced under the same process conditions. Following standard RCA- cleaning procedure, oxidation and annealing of samples were carried out in wet O_2 ambient at 1000 °C in a resistively heated furnace for 170 minutes. The oxide layer grown on Ge-implanted Si is slightly thicker than that on pure Si. This is consistent with what was observed in the wet oxidation of SiGe layers. The grown oxide

layers were made thick enough to ensure that the implanted layer is totally consumed during the oxidation process. Ohmic contacts on the backside were made by evaporating A1 and sintering at 600 °C under N_2 ambient for 15 minutes. Gate electrode of the diodes was formed directly by evaporating Al through suitable shadow masks with opening of diameter 1-1.3 mm. Low frequency and high frequency measurements were carried out using a Keithley 595 Quasistatic CV Meter, and an HP 4192A Impedance Analyzer.

3. C-V and G-V Characteristics

Figure 1 shows the high-frequency (HF), quasistatic (low-frequency, LF) C-V and G-V curves of the pure Si control sample. Figures 2 and 3 show the same as Figure 1 but for Ge-implanted samples, with implantation doses of $1x10^{15}$ cm^{-2}, and $1x10^{16}$ cm^{-2}, respectively. C-V and G-V curves of Si-MOS sample show the expected behavior of an ordinary MOS device, as shown in Figure 1. The theoretically calculated high frequency C-V and G-V curves are also added to Figure 1 for comparison. The accumulation and depletion parts are almost frequency independent while the inversion part shows frequency sensitivity at lower frequencies, as normally observed in MOS devices. The observed shifts in the curves relative to the expected theoretical curves are in the negative bias direction and related to the fixed positive oxide charge, which amounts to $7.6x10^{11}$ charges/cm^2 in the sample shown in Figure 1.

Unlike the Si-MOS capacitor, the C-V and G-V curves of Ge-implanted samples do not posses the properties of an ordinary MOS diode, as can be seen from Figures 2 and 3. They are frequency dependent at all biases and frequencies applied. A regular Si-MOS capacitor shows no frequency dependence in the accumulation region and a frequency dependence in the inversion region is observed if the minority carriers can follow the AC signal partly. This is what we obtained in our pure Si sample. The capacitance measured in the accumulation region of Ge-implanted samples is much lower than the oxide capacitance. As the frequency of the measurement decreases, the capacitance increases. It is seen that the frequency dependence gets weaker in the low frequency region, and it approaches the QS capacitance value in the inversion side of the curve. QS capacitance value represents the oxide capacitance. Since the identically processed Si sample did not exhibit this anomaly, the observed C-V and G-V curves and their frequency dependence should be related to the electrical properties of the interfaces of Ge-implanted samples.

4. A Model for the SiO_2/SiGe/Si Structure

The C-V curves of Ge-implanted samples exhibit substantial differences from those of pure Si sample, as presented in the previous section. The major difference is seen in the accumulation side (for negative biases) as a frequency dispersion. This can not be related to a series resistance effect of the substrate and/or ohmic contacts because identically processed Si samples do not show such frequency dependence. The observed characteristics of Ge-implanted samples can be explained by considering the new electronic band structure formed after the implantation and oxidation. As discussed briefly in the previous sections, a Ge-rich layer is formed at the interface after the oxidation.

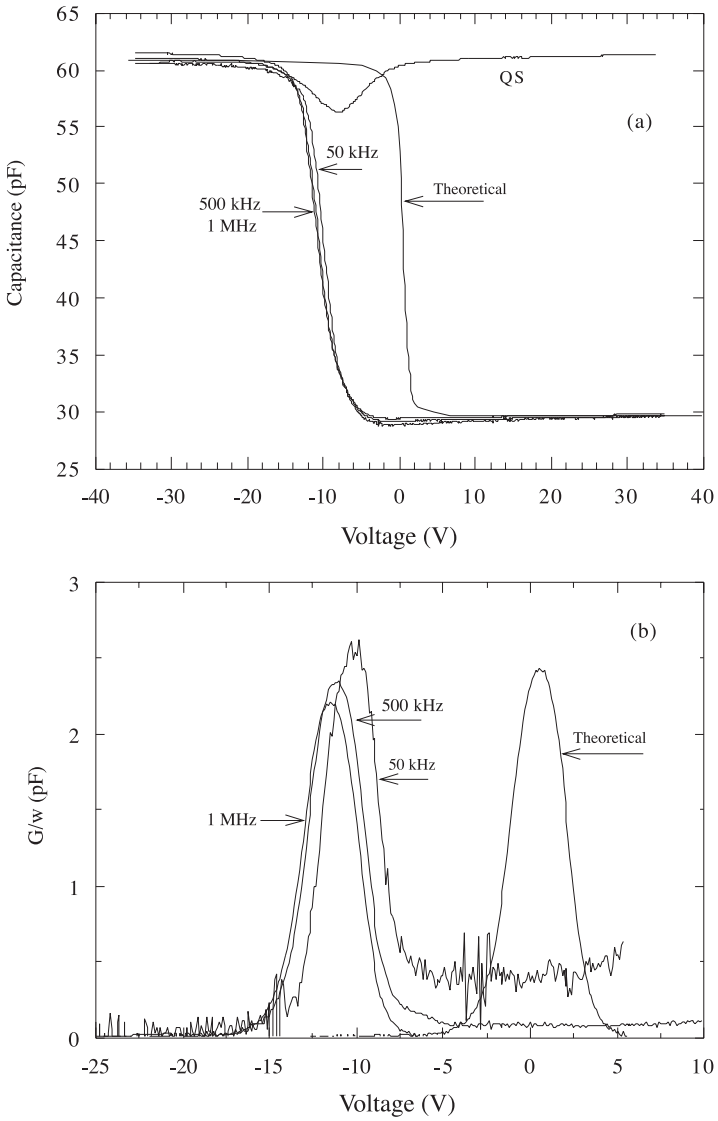

Figure 1. (a) C-V and (b) G-V characteristics of the pure Si sample. Process conditions are identical to the Ge-implanted samples.

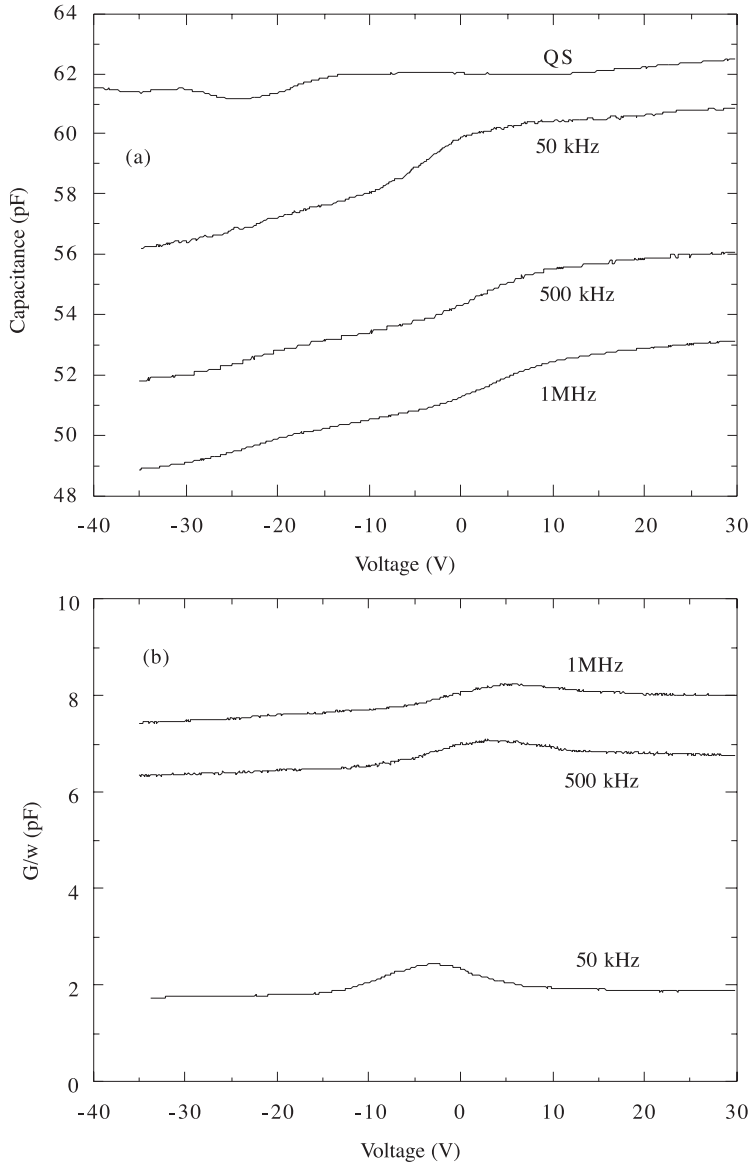

Figure 2. (a) C-V and (b) G-V characteristics of the sample which has an implantation dose of $1x10^{15}$ cm^{-2}.

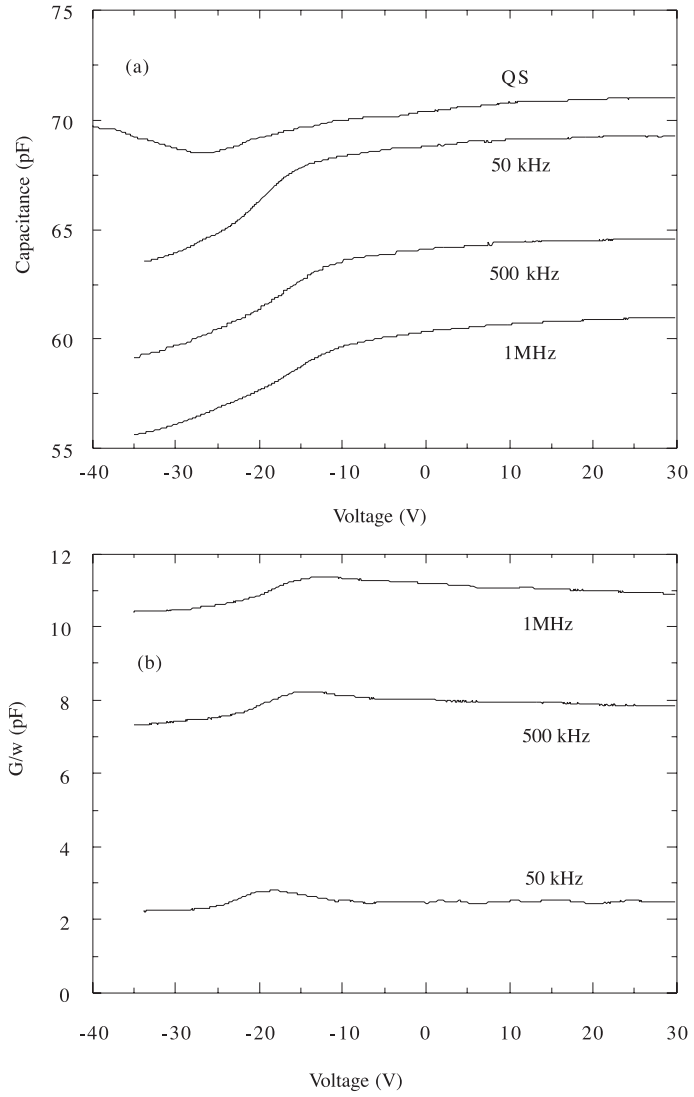

Figure 3. (a) C-V and (b) G-V characteristics of the sample which has an implantation dose of $1x10^{16}$ cm^{-2}.

The possible band profile of the new interface is schematically shown in Figure 4 (a). It is known both experimentally and theoretically that that the band edge discontinuity in the conduction band is negligible. It is assumed to be zero in this work. The discontinuity in the valence band is then equal to band gap difference. The interface at the SiGe/Si junction may not be as abrupt as indicated in Figure 4(a) due to the Ge distribution after

the implantation and oxidation. Also, the strain in SiGe layer due to the pseudomorphic growth on Si substrate and the presence of SiO_2 makes the electronic structure more complicated than given in Figure 4 (a). However, this model reflects the essential properties of the interface for the treatment given below. In addition to the new band structure formation, one may expect the presence of various defects at the interface. These defects may have resulted from ion implantation and/or lattice mismatch between SiGe and Si substrates. These defects may act as active trapping centers for the charge carriers.

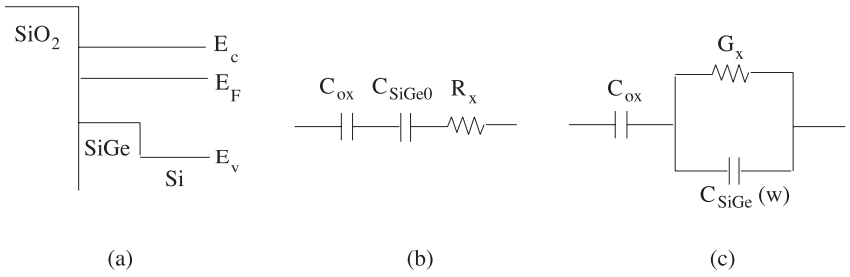

Figure 4. (a) Schematic electronic band diagram for $5i0_2$/SiGe/Si structure, (b) Equivalent circuit for MOS produced on Ge-implanted Si. c) Same as b) but drawn in parallel mode.

The essential feature of this band structure model is that a quantum well and/or trap region is formed for holes in the valance band. The potential barrier (band-offset) formed between SiGe layer and Si forms a resistance against the movementof holes in this region. The majority carrier (hole) response may then be expected to be small in these samples. In addition, if the holes are trapped by the trap states which may amount to high values an additional delay time may be expected due to the process of trapping and untrapping. As a result, the majority carriers may not follow the measurement signal, resulting in frequency dispersion observed in the accumulation part. The MOS capacitors produced on n-type samples was successfully explained by this model previously [20]. In n-type samples frequency dispersion was not observed in the accumulation side, because the majority carriers do not experience any potential barrier in the conduction band. The equivalent circuit corresponding to the band structure model is shown in Figure 4 (b). Here, R_x is the resistance associated with the electronic barrier during the exchange of carriers between the states in SiGe and Si substrate. Other resistive contributions are neglected.

The admittance associated with the SiGe part can be found by adding the impedances and taking the reciprocal of the resultant impedance:

$$Y_{SiGe} = \frac{1}{Z_{SiGe}} = \frac{1}{R_x + \frac{1}{j\omega C_{SiGe_0}}} = G_x + j\omega C_{eq} \tag{1a}$$

$$Y_{SiGe} = \frac{\omega^2 C_{SiGe_0}^2 R_x}{1 + \omega^2 C_{SiGe_0}^2 R_x^2} + j\omega \frac{C_{SiGe_0}}{1 + \omega^2 C_{SiGe_0}^2 R_x^2}, \tag{1b}$$

where ω is the frequency of the measurement, C_{SiGe_0} is the capacitance of the SiGe layer at zero frequency. The corresponding band diagram is shown in Figure 4(c).
According to this model, capacitive contribution of SiGe layer and/or defects related to the Ge implantation is strongly frequency dependent, i.e.,

$$C_{SiGe}(\omega) = \frac{C_{SiGe_0}}{1 + \omega^2 C_{SiGe_0}^2 R_x^2}. \tag{2}$$

In above equation, two limiting conditions are as follows:

$$\text{as } \omega \to \infty, C_{SiGe} \to 0$$

$$\text{as } \omega \to 0, C_{SiGe} \to C_{SiGe}.$$

Since the thickness of the SiGe layer is very small, as w C_{SiGe_0} may be expected to be large compared to oxide capacitance. The effect of SiGe is then negligible at zero frequency. Thus the measured capacitance approaches the oxide capacitance at low frequencies. This model explains consistently the experimental observations in the accumulation region. In an ordinary Si-MOS capacitor, accumulation capacitance is equal to the oxide capacitance. In the present case, an electronic barrier resulted from SiGe formation and trap states causes the majority carriers (holes) to delay in responding to the measurement signal, resulting in a smaller capacitance. At low frequencies majority carriers can follow the signal and the measured capacitance approaches the oxide capacitance value. The inversion regions of C-V curves can be explained in a more straightforward manner. Since no band edge discontinuity is expected in the conduction band, minority carrier behavior is not expected to be different from those of an ordinary Si-MOS capacitor. In fact, the MOS capacitors produced on n-type Ge-implanted Si samples yielded normal C- V curves without an anomaly [20]. However, a strong frequency dispersion is observed in the inversion region. This can be interpreted as the normal minority carrier behavior, because they can follow the high frequency signal due to high generation rate. High generation rate may be expected because of low band gap and high density of generation centers at the interface.

The conductance-voltage (G-V) curves should also be explained. G-V curves have the same frequency dispersion for all applied biases. They shift up almost parallel with the frequency. The accumulation side of the G-V curves can be described by the model described above. Equation (1) predicts that the conduction should increase with increasing frequency, and this is what is seen in Figures 2 and 3. The inversion side of the G-V curves has the frequency dispersion due the high minority carrier generation rate. In the G-V curves of Ge-implanted samples, a weak peak was observed as seen in Figs. 2 and 3. Taking the quasi-static curves as reference, the positions of these peaks are not within the depletion region. Secondly, the peaks shift towards the positive biases with increasing frequency; in a Si-MOS capacitor conductance peak shifts in the negative bias direction as observed in the sample produced in this work, Figure 1. This indicates that the observed

peak of Ge-implanted samples may have resulted from the interaction between minority carriers and the states at the interface.

Finally, the effect of implantation dose on the properties of the MOS capacitors should be addressed. It is seen from Figure 2 and Figure 3 that the C-V and G-V curves have generally the same features for two different doses. This shows that a dose of $1x10^{15}$ cm^{-2} is enough to create the band profile and the electronic structure presented above. It may be reasonable to assume that the essential features of the electronic structure do not change by adding more Ge to the Ge-rich layer. The only significant difference between these samples is the position of the dip of the QS curves. We see that the dip for the sample with the higher implantation dose is at a more negative potential than the sample with lower implantation dose. This indicates that the amount of positive charge, which causes the shift in the negative direction, increases with the dose of implantation. This is likely to result from the increase in trap density with the implantation dose. In summary, it was shown that the properties of MOS capacitors produced on a p-type Ge-implanted Si are fundamentally different than those of a pure Si substrate. The major difference was that the accumulation side of the C-V curves was strongly frequency dependent for the Ge-implanted Si. This frequency dispersion was attributed to a delay in the majority carrier response due to the presence of a quantum well and trap states associated with the SiGe formed during oxidation. An equivalent circuit model, which include the presence of the SiGe layer and a potential model was used to describe the observation.

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