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Barrier Heights of Antimony / and Bismuth / P-Silcon (100) Junctions

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Abstract

Junctions were fabricated in vacuum of about 10^{-5} Torr by thermal evaporation of Sb or Bi onto chemically etched p-type silicon (100) substrates. The electrical properties were studied by current voltage (I-V) measurements. Some of the Sb and Bi junctions were heated-treated for $\frac{1}{2}$ hr at 200 and 150°C, respectively. The barrier height (BH) was equal to 0.64 eV for both as-deposited and heat-treated Sb junctions, while it was 0.56 and 0.74 eV for as-deposited and heat-treated Bi Junctions, respectively. These observatimons indicate that for Sb junctions, annealing at a temperature of 200°C resulted only in partial elimination of any interfacial layer (oxide), while it modified the density of interface states. On the other hand, for Bi junctions, heat-treatment at 150°C eliminates completely the oxide layer, while also modifying the density of interface states.

1. Introduction

The discovery of rectification stimulated interest in the study of contacts between materials. Foremost in this regard is the extensive work which had been reported on the p-n homo-and hetero-junctions [1-3], metal semiconductor (M-S) junctions [4,5] and more recently, amorphous-crystalline semiconductor junctions [6-8]. By comparison, very little is known about metalloid-elemental semiconductor junctions [9-11], while some structure related interface studies have been reported on metalloid/III-V system [12-17]. Such studies were sometimes aimed at advancing knowledge on hetero-epitaxial growth. We note however that the amorphous-crystalline semiconductor junctions have been described as behaving more or less like the M-S junctions [6-8]. On this basis, one would expect the

metalloid-semiconductor junctions to also behave like M-S junctions, the degree of such similarity is yet to be fully established.

Studies carried out on the metalloid Sb and Bi have shown that metallic character increases from Sb to Bi [18]. Crystalline Sb [19] and Bi [20,21] are described as semimetals with small band overlaps (about 25 meV for Sb). On the other hand, Sb films are described as amorphous and semiconducting with a pseudogap comparable to that of amorphous Ge (that is, about 0.66 eV) and with a conduction mechanism of thermally activated hopping between localized states [19], while Bi films are described as polycrystalline as well as semiconducting [21,22].

The nature of a metalloid/semiconductor contact is by no means predictable. For the Sb/GaAs(110)[12] and Sb/InP(110)[11] contacts, each with 1 monolayer (ML) Sb coverage, the interfaces have been described as unreactive, abrupt and exhibiting high resistance to oxidation. On the other hand, depending on the annealing temperature, up to three phases have been reported in the surface reaction at the GaAs(001)/Sb interface [14]. Also, while experimental studies [9,15,17] suggest that for up to 1 ML Sb deposition, the Sb/GaAs(110) interface is semiconducting with no occupied Sb surface states lying within the fundamental energy gap of the GaAs(110) system, theoretical calculations [16] have predicted metallic interfaces arising from a partially occupied peak at the Fermi level which lies within the fundamental energy gap of the GaAs(110) system. It is further reported [9-11] that during the formation of Sb/InP(110) contacts, the first Sb monolayer on the InP(110) substrates is crystalline, with additional deposition being amorphous, and finally again becoming crystalline beyond about 15 monolayers at room temperature. The Sb/n-InP(110) junction is described as ohmic, and the Sb/n-InP(110) junction as a high barrier (∼1.1 eV) rectifier [11]. For Bi contacts, Kumar et al. [23] have reported on the doping of p-type As_2Se_3 with Bi to obtain n-type As_2Se_3:Bi which served as substrate in the fabrication of a Bi/n-As_2Se_3:Bi Schottky barrier solar cell.

Structural studies [24,25] carried out on the Bi/Si interface have identified two structures (1×2 and 2×2 phases) in the adsorption of Bi on Si(001) surface, while an additional disordered Bi component was also identified at 0.2 ML coverage of Bi on Si (001) [25] between room temperature and 420 K.According to Qian et al [25], after annealing to 520 K,about 50% of the disordered Bi and 10% of the 2×2 phase were converted into the 1×2 phase, The extent to which such varied changes in the nature of the metalloid contact influence charge transport across the interface has yet to be established.

We present in this work the current-voltage characteristics of Sb/and Bi/p-Si(100) contacts from which we have determined the barrier heights by two different methods. One method was by forward extrapolation of the linear (Schottky) part of the InJ-V characteristics to zero bias voltage, which gives [5] the hole BH as

$$\phi_B = -\frac{kT}{q} \ln[J/J_o A^\star T^2]. \qquad (1)$$

The other method was by forward measurements derived from plotting

$$F(V) \equiv \frac{V}{2} - \frac{kT}{q} \ln[J(V)/A^{\star}T^2] \tag{2}$$

against V, which gives [26] the BH as

$$\phi_B = F_m + V_m/2 - kT/q, \tag{3}$$

where F_m is the minimum of $F(V)$ at $V = V_m$. We have also analysed the nature of the interfaces.

2. Expremintal Procedure

The p-type silicon wafers, of orientation (100), resistivity 5 Ω-cm and 250 μm thick, were first degreased with soap and clean water, and then with trichloroethylene vapour, before being boiled for about 3 minutes in nitric acid of concentration 65% and again rinsed in clean water. This was followed by ultrasonic cleaning in trichloroethylene, acetone and alcohol, in that order. Then the wafers were etched in CP6 solution, rinsed with distilled, de-ionized water and blow-dried with nitrogen gas, and thereafter mounted on clean metal masks and in which they were immediately transferred to the chamber of an Edwards model 306 coater. The chamber pressure was subsequently maintained at about 10^{-5} torr with an oil diffusion pump backed by a rotary vacumm pump.

Films of Sb or Bi, of nominal purity 5N9 (Ventron,Germany), measuring 800 $\AA$ thick for Bi contacts and 1000 $\AA$ thick for Sb contacts were deposited by thermal evaporation onto the p-silicon substrates. Some of the Sb contacts were annealetd in vacumm at 200°C, while some Bi contacts were annealed at 150°C. The annealing time was 30 minutes.Ohmic contacts of Al, about 800$\AA$ thick, were deposited onto both the as-deposited and annealed Sb and Bi films, while In(Hg) contacts were afixed [27] to the back of the p-Si(100) substrates. All film thicknesses were determined by an Edwards model FTM3 Film Thickness monitor, while film cross-sections were determined with a travelling microscope. The overall diode structure and dimensions are as shown in Figure 1.

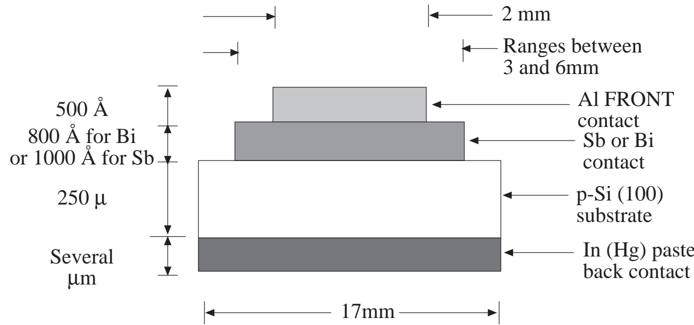

Figure 1. Structure of Diode Samples.

Current-voltage measurements were taken at room temperature with the test diodes mounted inside an electrically screened chamber which was maintained under vacuum of about 10^{-4} torr.

Results

The forward J-V characteristics for both as-deposited and annealed Sb/and Bi/p-Si(100) junctions are shown in Figure 2, from which the effects of recombination and series resistance can be seen. The reverse data are displayed in Figure 3 which exhibits, over varying voltage intervals, clear current saturation regimes where Schottky current component dominates. These are followed by soft breakdown. Thus both figures show that the contact are rectifying. BH values which are determined from both forward extrapolation to zero bias [5] and Norde [26] plots are displayed in Table 1. The figures also show that for Sb and Bi contacts, forward current decreases upon annealing at 200 and 150 °C, respectively, while reverse current decreases for Bi contacts and increases for Sb contacts upon annealing.

Table 1. Barrier Heights of filament-evaporated Sb and Bi contacts to p-Si (100) substrates.

(All substrates were of resistivity 5 Ω-cm and were chemically etched prior to metalloid contact deposition.)

Diode Structure	Diode Name	Junction State	Junction Area (cm^2)	Contact Thickness (Å)	Hole Barrier Height ϕ_B (eV) By forward extrapolation [5]	Hole Barrier Height ϕ_B (eV) By Norde plot [26]
Al-Sb/pSi-In(Hg)	D1	As-deposited	0.27	1000	0.65	0.64
Al-Sb/pSi-In(Hg)	D2	Annealed at 200° C for $\frac{1}{2}$ hr	0.15	1000	0.64	0.64
Al-Bi/pSi-In(Hg)	D3	As-deposited	0.08	800	0.57	0.56
Al-Bi/pSi-In(Hg)	D4	Annealed at 150° Cfor $\frac{1}{2}$ hr	0.27	800	0.75	0.74

Discussion

The effects of recombination and series resistance are clearly discernable in the forward current (Figure 2) which shows departures from Schottky-like behaviour below 0.08 and above 0.2 V, respectively. The recombination occurs in the depletion region, within the oxide (SiO_2) layer which automatically develops as a by-product of the chemical etching process, and at the localized states (interface states) on the SiO_2/or metalloid/Si interface. Also, the SiO_2 layer present additional resistance which takes up part of the applied diode voltage. However, the influence of these effects has been minimized by our methods [5,26] of determining the BH values displayed in Table 1.

Similarly, we attribute the general rise of reverse current with voltage (Figure 3) partly to contribution of bulk, edge and surface generation current, each of which is known to increase with voltage as $V^{\frac{1}{2}}$ and partly to barrier lowering both from image force effects which varies as $V^{\frac{1}{4}}$ [4], and from the modified band-bending in the Si substrate due to the presence of interfacial layers between the substrate and the metalloid contact.

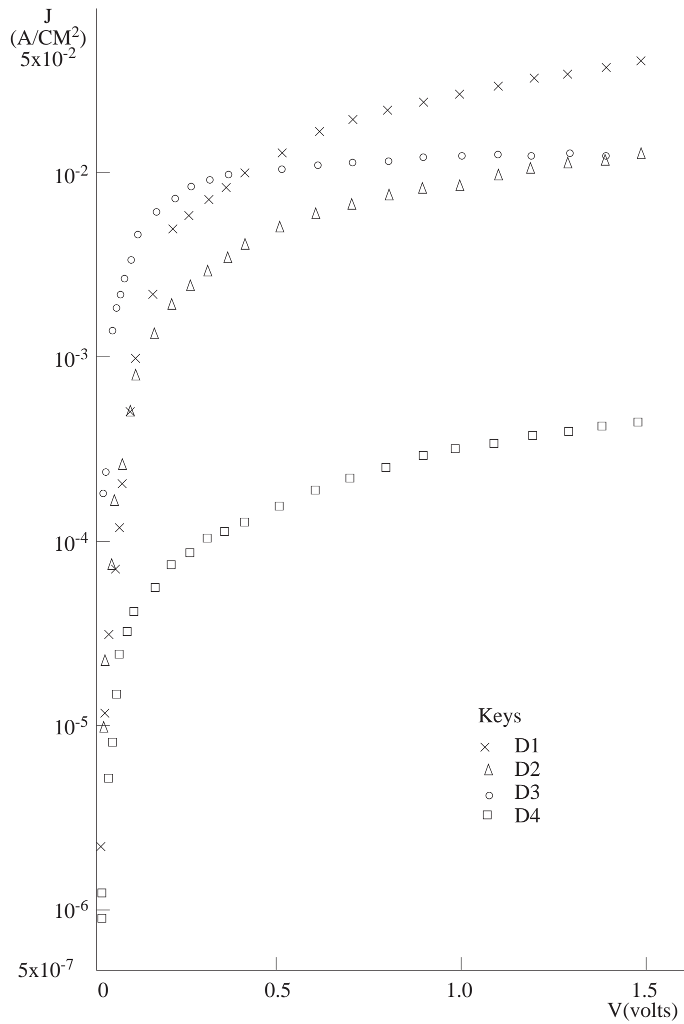

Figure 2. Forward J-V Characteristics for un-annealed (D1) and annealed (D2) Sb/p-Si(100) contacts, and for un-annealed (D3) and annealed (D4) Bi/p-Si(100) contacts at room temperature.

Figures 2 and 3 also show that heat-treatment leads to decrease in both diode forward and reverse currents for Bi junctions. For Sb junctions, however, heat-treatment causes the forward current to decrease while the reverse current increases. In addition, Table 1 shows that while heat-treatment does not change the BH of 0.64 eV for Sb junctions, it causes BH to increase from 0.56 to 0.74 eV for Bi junctions. These observations are attributable in part to the influence of the SiO_2 layer which is sandwiched between the

metalloid and the p-Si substrate (Figure 4), and which takes up part of the applied voltage, and in part to the presence of the localized states within the oxide layer and at the SiO_2/Si interface in the case of unannealed and annealed Sb and unannealed Bi contacts (Figures 4(a), (b) and (c)), or localized states at the metalloid/p-Si interface for annealed Bi contracts (Figure 4(d)). It has been reported that the use of HF to remove silicon oxides on the surface of silicon invariably leads to hydrogen (from the HF) termination of the dangling bonds on Si, and that this reduces surface gap states on n and p-Si(100)[28].

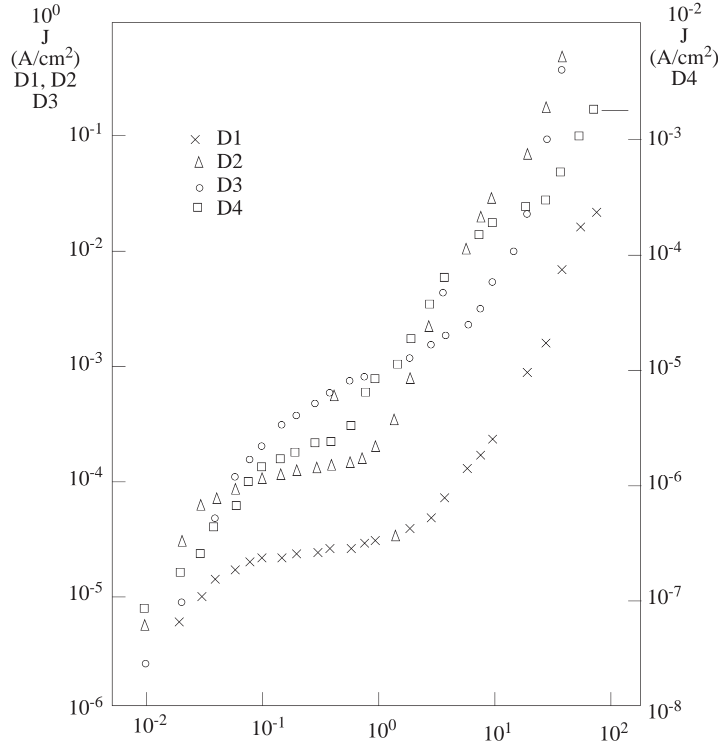

Figure 3. Reverse J-V characteristics for as-deposited $(D1)^{V(V)}$ and annealed (D2) Sb/p-Si (100) contacts, and for as-deposited (D3) and annealed (D4) Bi/p-Si (1000) contacts at room temperature

It appears that for our Sb contacts, the annealing temperature of 200 °C (Sb melting point is about 630 °C) is inadequate to cause appreciable diffusion of Sb atoms through the native SiO_2 layer and make it disappear completely. We are therefore left with a reduced layer of SiO_2 between the Sb and p-Si (Figures 4(a) and (b)). Yapsir et al [29] have had to go up to 450 C in order to break the oxide and form a good contact between

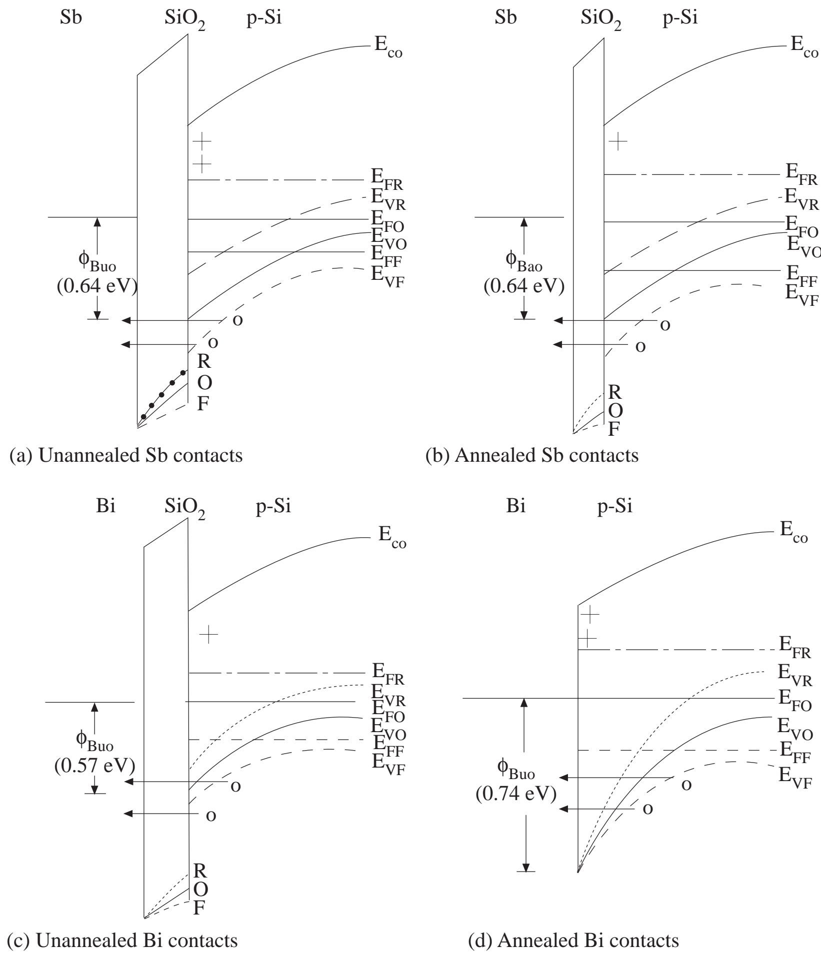

Figure 4. Proposed energy band picture for Sb and Bi contacts to chemically etched p-Si (100) substrates. (Annealing temperatures are 200 C for Sb and 150 C for Bi contacts. E_V and E_C are, respectively, the valence & conduction band edge, and E_F is the Fermi level. The letters O,F,R, when used either in isolation or as subscripts refer, respectively, to zero, forward and reverse bias. $\phi_{\rm Buo}$ and $\phi_{\rm Bao}$ refer to the BH of the unannealed contacts, respectively. + denotes positively charged interface states; while ++ is denser than +).

A1(melting point about 660 °C) and n-Si. Also, for our Sb contacts, the annealing would invariably result in a reduced density of the SiO_2/p-Si interface. While the reduction in the SiO_2 layer leads to an increase of both the BH and the depletion layer width (w) and hence the band bending ($\propto w^2$), the reduced density of interface charges however reduces both the BH and the depletion layer width and hence the band bending. These opposing

effects appear to cancel out each other and leave the BH more or less unchanged. Hence the BH value of 0.64 eV obtained for both as-deposited and annealed Sb contacts to p-Si in the present measurements. Under non-zero bias, and as a result of the reduced width of the SiO_2 layer in the annealed Sb contacts, the Si substrate now experiences more of the applied voltage which causes E_F to shift more than in the unannealed case. Such shift of E_F, coupled with the shift in the top of the valence band edge at the SiO_2/p-Si interface which also makes Ev of the p-Si substrate at the interface to shift, is sufficient to account for the observed reduction in forward current and increase in reverse current of the annealed Sb contact samples relative to those of the unannealed samples.

On the other hand, for Bi contacts, the annealing temperature of 150°C (Bi melting point is about 270°C) is enough to drive inward the Bi atoms through the intervening SiO_2 layer, which eventually disappears, leaving behind a Bi/p-Si junction with its own characteristic interface states. In order to adequately explain our present results, we would have to assume a higher density of positively charged Bi-related interface states at the Bi/p-Si interface than those at the SiO_2/p-Si interface of the unannealed Bi contacts (Figures 4(c) and (d)). Like the disappearance of the SiO_2 layer, the increased density of interface states makes both the BH and the width of the depletion region to increase as observed in our present work. Some reports have stated that a native oxide (such as SiO_2) of thickness 15-20 $\mathring{A}$ can stand field strengths as high as 10^7 V/cm [30], and that positive charge in the oxide can increase hole barrier heights by several tenths of a volt for contacts to p-Si solar cells [31]. Thus, the observed increase of BH of the Bi/p-Si junctions from 0.56 eV for the unannealed case to 0.74 eV for the annealed case appears to be reasonable. Increases of BH by about 0.1 eV upon annealing above 450°C has been reported for A1/n-Si contacts [32], while BHs of some metal contacts to p-Si substrates have been known to either increase or decrease due to decrease in the density of interface states [33,34]. Under non-zero bias, and as a result of the disappearance of the SiO_2 layer in the annealed Bi contacts, the Bi/p-Si junction now experiences all the applied voltage, less the drop over the bulk series resistance of course, thus making E_F to shift much more than in unannealed case. Such shift of E_F, coupled with the increased BH, result in decrease of both forward and reverse current relative to the unannealed case, as has been observed in our present result for Bi contacts to p-Si(100).

Our results indicate that Sb/and Bi/p-Si interfaces behave like m-s interfaces. This assertion goes along with the M-S interfaces predicted from theory for Sb/GaAs(110) interfaces [16], but contradicts the semiconductor-semiconductor interfaces predicted from experiments [15] for the same Sb/GaAs(100) interfaces.

3. Conclusion

Current conduction across Sb/and Bi/p-Si(100) junctions is strongly dependent on the mode of Si substrate surface treatment prior to metalloid deposition and also on post-deposition annealing. The sample preparation technique by chemical etching produces a thin SiO_2 layer between the metalloid and the Si substrate. The SiO_2/p-Si(100) interface contains localized states which are positively charged. Annealing $\frac{1}{2}$ hr at 200°C for Sb

contacts and 150°C for Bi contacts results in modification of the interfaces in such a way as to cause the contact BH to remain unchanged at 0.64 eV for Sb contacts, and to increase from 0.56 to 0.74 eV for Bi contacts.

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