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The Determination of Thermal Annealing Effect on the DOS Profile of a-Si:H Film

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Abstract

In this study the aim was to investigate the effect of thermal annealing on the density of states (DOS) of hydrogenated amorphous silicon (a-Si:H) by means of a Schottky structure. In order to realize that goal the sandwich structured Au/a-Si:H/a-Si:H(n^+-type)/Cr Schottky diode was fabricated. The junction capacitance of the samples were measured as a function of the amplitude of alternating voltage in the frequency range of 500 Hz - 100 KHz and in the annealing temperature range of 23 - 175° C. The density of states profile as a function of both annealing temperature and energy were plotted. The effect of the annealing on the density of states (DOS) is discussed.

1. Introduction

Reverse bias annealing experiments carried out on the Schottky and p/i/n type diodes showed that the annealing processes significantly changed their current-voltage and capacitance-voltage characteristics [1,2]. It has been reported that the source of the changes in the characteristics come mainly from the n^+-type layer [3,4,5,6,7,8,9]. One investigator reports that reverse bias annealing in phosphorus-doped a-Si:H increased the band tail electron density [10]. The experiments also confirmed that reverse bias annealing mainly enhanced the active donor density [11]. Also, it has been reported that thermal annealing increased the electrical conductivity of a-Si:H to a large extent and removed structural defects [12].

This work intended to investigate the effect of thermal annealing on the density of states (DOS) N(E) in the gap of hydrogenated amorphous silicon (a-Si:H). In order to make a contribution to the physical understanding, Schottky diodes formed in the Au/a-Si:H/a-Si:H(n^+-type)/Cr sandwich structure were fabricated and their current-voltage and capacitance-voltage characteristics were measured. In order to see the effect of reverse bias annealing on the diode characteristics, density of states (DOS) profiles were obtained from the capacitance-voltage characteristics before and after thermal annealing.

2. Theoretical Background

For a small alternating voltage applied across a junction the junction capacitance C_0 is given by [13]

$$C_0 = \frac{\epsilon A \rho_e}{\epsilon F_e + x_e \rho_e}, \tag{1}$$

where A, ϵ, F_e and ρ_e are the junction area, the dielectric constant, the electric field and the charge density at point x_e, respectively. The value ρ_e is given simply by the integral over the density of states:

$$\rho_e = \rho(E_e) = q \int_{E_c+E_e}^{E_f^0} g(E) dE. \tag{2}$$

If the peak to peak (p-p) value of the alternating voltage drive level δV is not zero it is obtained through higher order corrections to the junction capacitance. Specifically,

$$C = C_0 + C_1 \delta V + C_2 (\delta V)^2 \tag{3}$$

where C_0 is given by Equation (1) and

$$C_1 = \frac{\epsilon A \rho_e^2}{2(\epsilon F_e + x_e \rho_e)^3}. \tag{4}$$

The charge density N_{DL} was obtained from Equation (1) and Equation (4) as follows:

$$N_{DL} = -\frac{C_0^3}{2q\epsilon A^2 C_1} = \frac{\rho_e}{q}. \tag{5}$$

It is explicitly seen from Equation (5) that the charge density N_{DL} is directly and simply related to the density of states in the material $g(E)$ through Equation (2).

3. Experiment

The preparation of the devices was described in our previous paper (Serin 1987). At first the junction capacitance versus alternating voltage amplitude were measured in

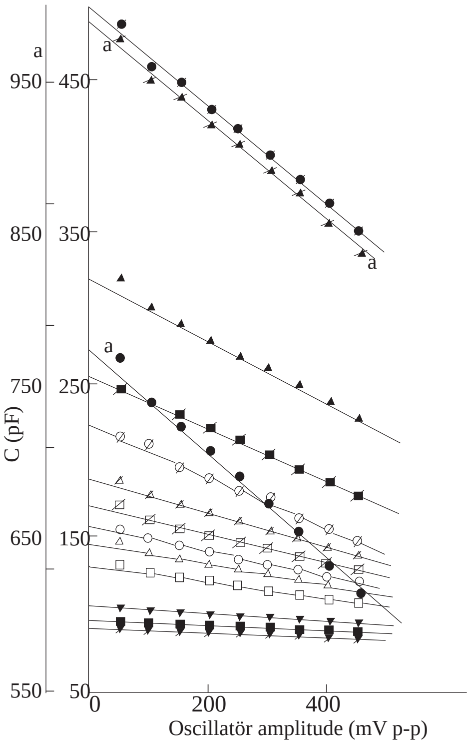

Figure 1. The capacitance-oscillator amplitude characteristics at 23° C for several values of frequency (KHz): (▲̸) 0.5, (●) 1.0, (●̸) 2.5, (▲) 5.0,(■̸) 7.5, (∅) 10.0, (△̸) 12.5, (☐̸) 15, (○) 17.5, (△) 20.0, (□) 25.0, (▼) 50.0, (■) 75.0, and (▼̸) 100.0

the frequency range 500 Hz - 100 KHz (which roughly corresponds to the energy range 0.35-0.50 eV) with peak voltage under 4 Volts at room temperature (see Figure 1). Then the sample was placed in an oven at 100° C for 30 minutes while a 2 Volts reverse bias voltage was applied to its terminals. After annealing the sample was left to cool to room temperature in the oven in the presence of the reverse bias. The same annealing processes were repeated at the annealing temperature 130° C, 150° C and 175° C. After the each annealing, the measurements of junction capacitance versus the amplitude of alternating voltage were repeated over the same frequency range in the same way mentioned above. For the each annealing temperature the variation of N_{DL} was determined at -4 Volts bias as a function of the frequency.

4. Results and Discussion

The measurements carried out at room temperature over the frequency range of 500 Hz - 100 KHz as a function of voltage (measured peak-to-peak) showed that the junction capacitance linearly decreased with increasing voltage. It was also observed that the junction capacitance decreased with increasing frequency. The thermal annealing measurements in the annealing temperature range of 100° C, 130° C, 150° C and 175° C showed that annealing processes significantly affected the junction capacitance (see Figure 1). The change in the capacitance by means of annealing explicitly exhibited that annealing processes created modifications in the density of states. In order to determine the effect of annealing on the DOS Michelson's drive-level profiling technique was applied to our results. For the measurement conducted at annealing temperature of 100° C the values of C_0 and C_1 were determined from the intercept and limiting slope of the straight lines characterizing the capacitance "peak to peak" voltage plot. The same processes were repeated for the annealing temperature of 130° C, 150° C and 175° C. In order to calculate the charge density N_{DL}, which simply related to the density of states in the material $g(E)$ through Equation (2), the values of C_0 and C_1 were used in Equation (5). The calculated DOS for various frequencies was plotted versus energy and the curves shown in Figure 2 were obtained. It was observed that the density of states curves first decreased with increasing energy to a minimum then increased with increasing energy. Thus the DOS was significiantly changed by means of thermal annealing.

Vieux [14], Balberg [15], Snell [16], Viktorovitch [17], Abram [18] and Winer [19] were among the researchers who recently pursued the determination of density of state profile. In their studies, capacitance-voltage-frequency or frequency-capacitance-temperature techniques had been used.

The method followed by us in te determination of density of states was Michelson's drive-level profiling technique. The main differences with Michelson's experiment come from the composition of the device structures. For example, our device was a Au/a-Si:H/a-Si:H(n^+-type)/Cr type Schottky structure while Michelson's devices were p^+-n junction and Schottky diodes with palladium. However, although the methods to determine the density of states, as a way to characterize the structures and the film preparation techniques, were different and the shape of density of states distribution were quite similar to the results of authors mentioned above.

In the present study, the second and the most original step was to determine the effect of the reverse bias thermal annealing on the density of states and on the shape of distribution. It can be generally said that the source of the changes in the density of states profile came from n^+-type layer [3,4,5,6,7,8,9]. Recent experiments using reverse bias annealing in phosphorus-doped a-Si:H [10] have also showed that band tail electron density increased. Possible mechanism for the increment of the band tail electron density n_{BT} were given as (a) an increase in $[P_4^+]$ by dopant activation and (b) a decrease in $[Si_3^-]$ centers. It was also shown that the defects or $[Si_3^-]$ centres were not affected by bias annealing. Since the depletion layer at low bias was characterized mostly by the shallow states, one can say that this layer is most sensitive to changes in the density of shallow states. Krötz and Müller's [12] experiments also confirmed that reverse bias annealing mainly enhances the active donor density. Hence they stated that doping of a-Si:H by means of annealing is best understood by the model of "autocompensation doping" [8,20].

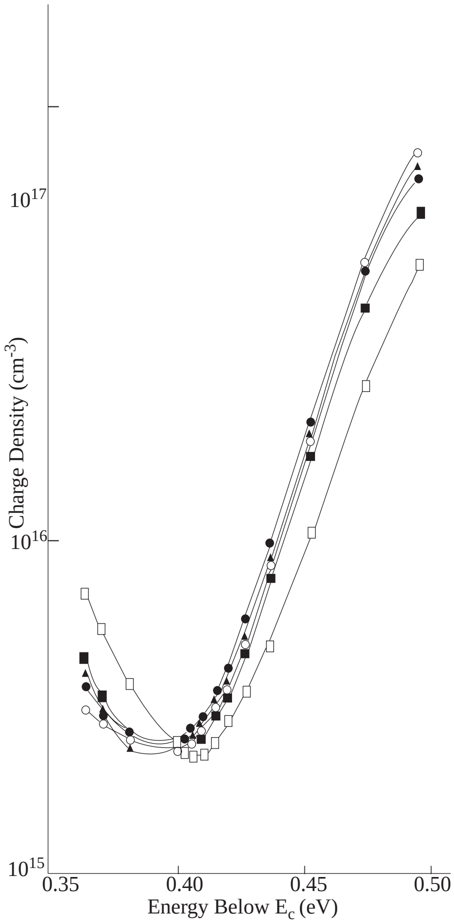

Figure 2. The plot of charge density N_{DL} versus energy below E_c for several annealing temperature (° C): (◯) 23, (△) 100, (•) 130, (■) 150 and (□) 175.

With help of the comments given above, the change in density of states profile by means of reverse bias annealing can be explained as follows. Each annealing processes at a different annealing temperature brings the n$^+$-type layer into a new thermal equilibrium. As the specimen is cooled in air to room temperature, hydrogen atoms easily changed their coordinations with both silicon and phosphorus by the release of hydrogen. This process breaks weak Si-Si or Si-P bonds [21,22,23,24]. When there is no external voltage on the specimen, the change in neutrality of shallow states n_{BT} can be defined as $[N_{Donor} - N_{DB}]$ where N_{Donor} and N_{DB} are the densities of donors and dangling bonds, respectively. It is obviously seen from Figure 2 that the number of dangling bonds N_{DB} decreased and with increasing annealing temperature and the band tail electron density n_{BT} increased with increasing annealing temperature. It was observed that these behaviors were in good aggrement with the relation $n_{BT} = [N_{Donor} - N_{DB}]$. As it was mentioned above, reverse bias voltage annealing differentiates our experiments from others. In this case, the expression for the charge neutrality n_{BT} is expressed by the equation $[N_{Donor} - N_{DB} - Q_{dep}/wq]$, where Q_{dep}, w and q are the depletion charge induced by the bias voltage, the width of the n^{+}-type layer and the electronic charge, respectively. The effect of annealing on the band tail electron density n_{BT} or on density of state profile is easily observed by means of the third term, Q_{dep}/wq. When the bias is removed at the end of each annealing process, n_{BT} increases by the amount of Q_{dep}/wq. As bias annealing is performed at the higher temperatures and for longer periods of time, the resulting n_{BT} increases by nearly two orders of magnitude. Thus the shape of DOS profile changes with increasing annealing temperature.

Finally, the results and their discussions of our experiment can be summarized as follows; the change in the density of states profile, as seen in Figure 2, by means of thermal annealing came from two sources. The first one was the decreament of dangling bonds N_{DB} due to annealing. The second was the changes of depletion charge (Q_{dep}) due to reverse bias annealing.

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