A Novel Single-Ended To Differential Converter In A High Bit Rate Clock And Data Recovery Input Circuit

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***Abstract* — Differential amplifiers respond with increasing phase difference between both outputs, when driven single-ended at high-speed. A novel asymmetrical delay-line was implemented between two stages to compensate this effect. This structure has been integrated in a clock and data recovery circuit (CDR) and measured on test chips.**

***Keywords* — Clock and data recovery, converters, delay-lines, differential amplifiers, group-delay, high-speed integrated circuits, jitter, MMICs, single-ended to differential conversion.**

I. Introduction

Signal converters from optical to electrical usually generate a single-ended electrical signal after the transimpedance amplifier (TIA). In case of very high-speed signals however, the use of differential signals on chip offers more advantages (e.g., current mode logic CML). The input buffer operates as single-ended to differential converter (SDC). The single-ended signal drives one input of a differential pair, whereas the second input of the differential pair is fixed at a reference potential (Fig. 1). For low and medium frequencies the differential outputs Y1 / YN1 show a good differential signal. At higher speed, however, the difference in delay and amplitude between both outputs Y1 / YN1 becomes more and more significant. This results in an insufficient eye opening and high jitter. The reason for this difference in performance is due to the different signal path lines from input (Gate M1) to the differential outputs (Drain M1, M2). M1 operates as common source circuit, but M2 as common gate circuit.

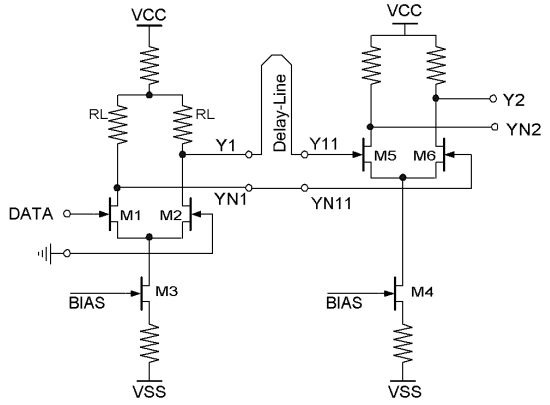

Fig. 1. Schematic of an SDC with asymmetric delay-line.

II. Design Method

Breaking the recommendation of fully balanced design for such high-speed circuits, a delay-line has been implemented asymmetrically in the signal path of Y1 between the first and the second differential pair (Fig. 1 and Fig. 3). The first expectation would be, to adjust the output YN1 (which would be expected to be earlier) by use of a delay-element to the later output Y1. But simulation has shown, that inserting the delay-line at the weak output Y1 solves the problem better (Fig. 2). The signals in front of the delay-line (Y1 / YN1) are shown in the upper diagram of figure 2. The DC levels of two consecutive signal crossings differ very much (e.g., at marker A, B). At marker A the voltage difference between Y1 and YN1 after crossing is quite poor. The signals behind the delay-line are shown in the lower diagram (Fig. 2). The DC levels of consecutive signal crossings differ less and the difference between Y11 and YN11 opens much better. Further simulations now predict a better signal and less jitter at the outputs Y2 / YN2 of the second differential pair, especially for fast signal changes after a long Low or High NRZ sequence.

Another theory to explain the positive influence of the delay-line could be the following: no perfect matching can be achieved between output Y1, delay-line and input of M5. An inductive part from the impedance of the delay-line seems to remain, compensating partly C_{Drain} of M2

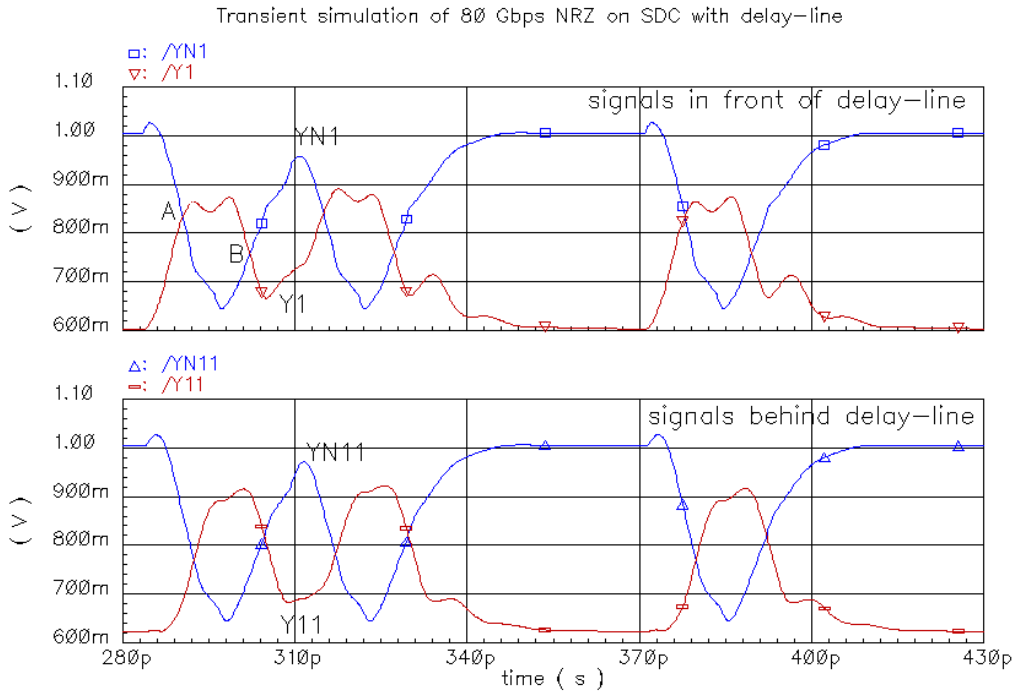

Fig. 2. Simulation result of an SDC with asymmetric delay-line.

and C_{Gate} of M5. This may cause a “peaking” and faster switching of the signal Y1 and Y11 (Gate M5).

III. Implementation

Test circuits have been designed in an MBE-grown-metamorphic-InGaAs/InAlAs-technology provided by the Fraunhofer-Institute for Applied Solid State Physics (IAF), allowing for 100 nm HEMT with an f_T of about 200 GHz [1], [2].

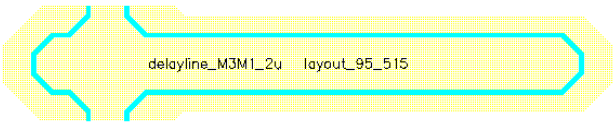

Fig. 3. Layout of an asymmetric delay-line with a delta in length of 420 µm (the chequered background represents the ground metal of the elevated micro strip line).

The delay-line consists of an elevated micro strip line of 2 µm width. This type of line is expected to show lowest attenuation at an impedance of the same order of magnitude as the load resistors (100 Ω) of the input differential pair. The metal layers for both ground-plane and micro strip line are carried out in gold. Figure 3 shows the layout of such a delay-line and its counterpart. The shorter one of both lines has the same bends as the longer one, in order to keep the same impedance for both. For the same reason the ratio "No. of pylons / air bridge length" is kept as similar as possible. Hence the two lines differ only in the extension of the horizontal parts.

To reduce the uncertainty caused by the not exactly known speed of signal propagation on this micro strip line we implemented several test chips with a variety of delay-lines differing in length. Again two groups of test chips were formed: group 1 with the load resistors of the input differential pair behind the delay-lines, group 2 with this load resistors in front of the lines.

IV. Measurements and Results

Figure 4a shows the measured group-delay of the reference chip. Figure 4b shows the group-delay of a chip with an asymmetric delay-line of 480 µm delta in length. This chip belongs to group 2, having the load resistors in front of the lines. Figure 4a and Figure 4b are typical for all test chips.

The difference in performance is evident. The delta in group-delay within the considered frequency range from DC up to 42 GHz is clearly less for the circuit with asymmetric delay-line, in this case 0.8 ps. In other words: the delta in group-delay within the considered bandwidth is about 20 % less compared to the conventional SDC.

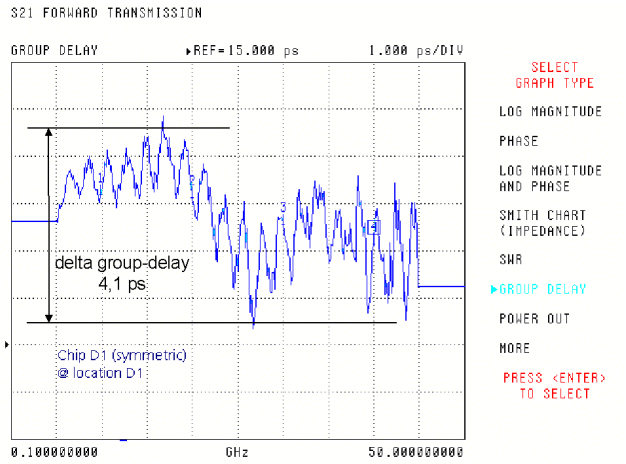

Fig. 4a. Group-delay of conventional SDC (reference chip).

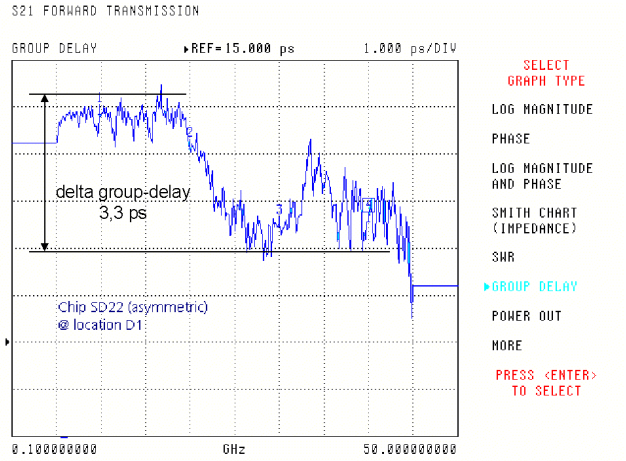

Fig. 4b. Group-delay of SDC with asymmetric delay-line.

Figure 5 summarises the delta in group-delay for all the measured circuits on one wafer. Circuit type "SD22" shows in average 0.7 ps less difference in group-delay within the considered bandwidth as the "conventional" reference structure “D1”. In addition, when compared with the chips from group 1 (R_{LOAD} behind delay-line) it indicates, that even for such relatively short "on chip" interconnects the load resistors before the line give better results, (i.e., reflections are more attenuated, [3]) than with the load resistors behind the line.

Less jitter in large signal behaviour on a PRBS or real data-signal may be expected, from the smaller difference in group-delay within the considered bandwidth.

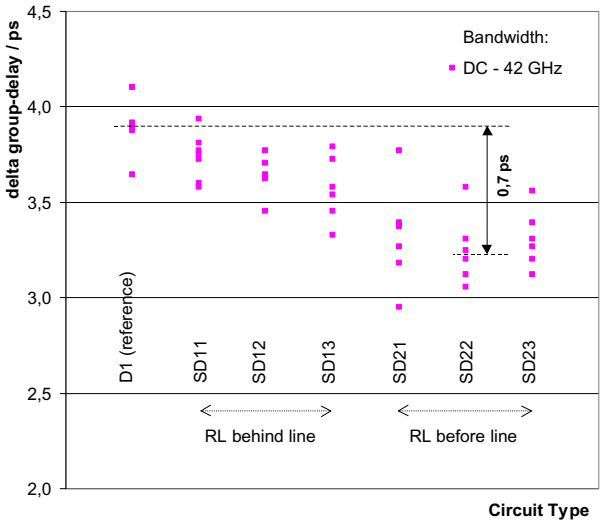

Fig. 5. Delta in group-delay within a bandwidth from DC to 42 GHz, measured for all seven circuit types placed on the same wafer (every dot represents one chip).

Simulations predict about the same amount of less jitter, as we have reduced difference in group-delay, (i.e., 0.5 to 0.75 ps). Measurements however indicated no detectable difference in jitter between the various circuit versions (Figure 6). The measurement set-up itself generated a jitter

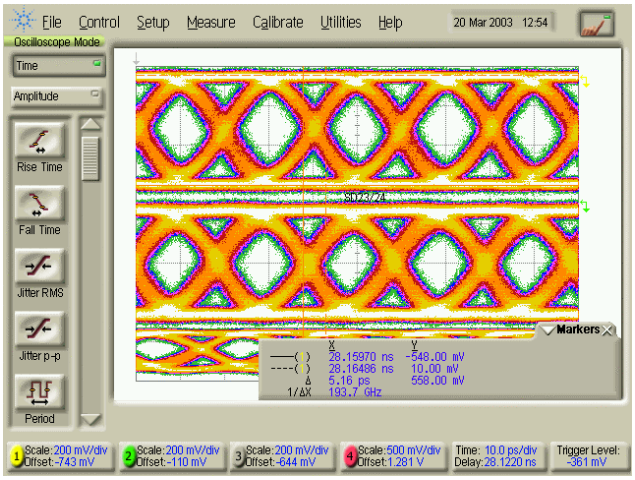

Fig. 6. Eye diagram at 50 Gbps, measured on an SDC of type “SD23” with asymmetric delay-line (up and middle: outputs, low: input).

of around 5 ps, which we think covers the estimated advantage in jitter between the conventional and the novel structure.

V. Application

The structure pursuant to type "SD22" has been implemented as data input buffer on a chip, belonging to a 80 Gbps clock and data recovery circuit (CDR). This chip works as Alexander Phase Detector [4]. The layout is shown in Figure 7. Measurements are currently under progress and look promising.

VI. Conclusion

The delta of group-delay in high-speed single-ended to differential data converters can be reduced with an asymmetric delay-line. This could become an interesting method to minimise the overall jitter in future high bit rate systems.

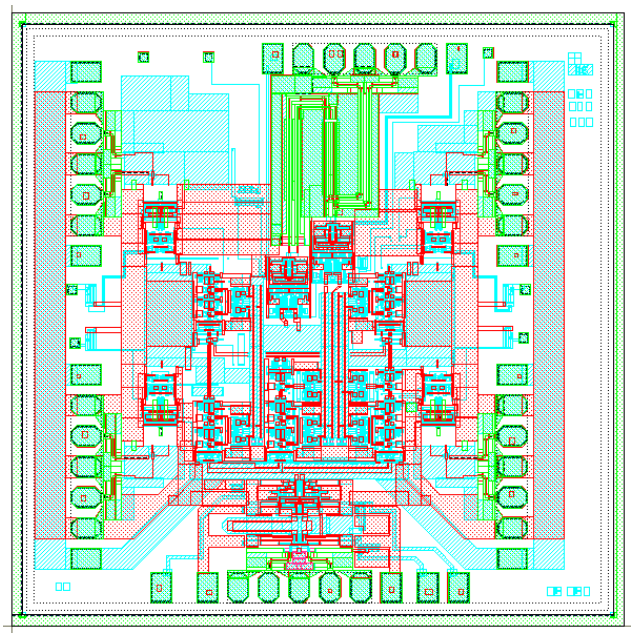

Fig. 7. Chip layout for a CDR component, using an SDC with asymmetric delay-line (at the middle, lower part of the picture).

Moreover this work indicates, that in very high-speed integrated circuits, the propagation delay on lines may offer new design utilities. The development of line models with a good prediction of delay and impedance, will be a challenge on this.

Acknowledgements

The authors would like to thank Arnulf Leuther[2] for helpful indications on the technology, Otmar Kappeler[2] for details about modelling, Oliver Weiß[1] and Manfred Ludwig[2] for the great support in measurements. Funding of the present work by the German Federal Ministry of Education and Research (BMBF) within the project "IC80G" is gratefully acknowledged.

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