Design of High-Speed CMOS ICs for 10 Gbit/s Optical Communication System

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***Abstract*— In this paper, the intrinsic disadvantages of the nowadays low-cost deep-submicron digital CMOS technologies in respect of the design of high-speed optical communication (OC) systems front-end integrated circuits (ICs) have been discussed. The critical passive components such as on-chip inductor and varactor, and the key high-speed circuits of clock and data recovery circuit (CDR) such as voltage controlled oscillator (VCO), data decision (DEC) and frequency divider (FD) for SDH/SONET level STM64/OC192 applications have been investigated.**

The satisfying results have been obtained from chips fabricated in a 0.18-μm standard CMOS process.

I. Introduction

Nowadays, the advanced deep sub-micron CMOS technologies have been capable of realizing the GHz ICs in the optical communication system front end. Nevertheless, to realize high-speed and high-performance analog circuits the intrinsic disadvantages of the deep-submicron digital CMOS technologies had to be overcome, which include the lack of the high-performance passive components and low operating voltage.

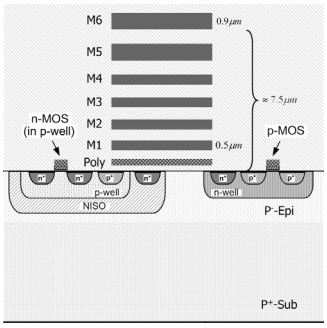
This paper presents the optimization of the on-chip passive components and the design of the key high-speed circuits with a 0.18-μm standard digital technology, which are intended for SDH/SONET level STM-64/OC-192 applications.

The paper is organized as follows. Section II provides a brief overview of a typical digital CMOS process. Section III and IV focus on the design of the passive components, i.e. the inductors and the varactors. 10 GHz voltage controlled oscillators (VCOs) that used the optimized passive components are presented in Section V. In Section VI the design of the data decision (DEC) and the frequency divider (FD) is discussed. Section VII demonstrates a new concept for a high-speed data decision with a feedback loop (DFL) for cancellation of inter-symbol interferences (ISI). Finally, conclusions are drawn in Section VIII.

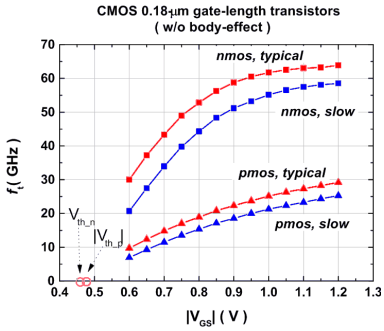
II. Deep Submicron CMOS Process

CMOS technology has emerged as the top solution due to its performance improvement by continuous scaling-down, ease of integration for digital and analog circuits and its cost advantage. Nevertheless, the shrunken voltage headroom caused by the simultaneous scaled supply voltage and the lack of high-performance passive components limit its high-speed analog applications.

The CMOS technology we used is a deep submicron standard technology with 0.18-μm feature size, 1.8 V supply voltage and cut-off frequency of about 50 GHz. As shown in the cross section of the process (Fig.1a), it has a epitaxial substrate with low bulk resistivity of 10^{-2} Ω·cm for the mitigation of latch-up effect. Six-layer thin aluminum metalization and thin dielectric ($\varepsilon_r \approx 4.2$) for high wiring density and deep nwell (NISO) for isolation are available.



(a) Process cross section



(b) Cut-off frequency of FETs

Fig. 1. 0.18-μm digital CMOS technology

Despite scaling-down and the performance improvement, the digital CMOS technology has still some problems for super high-speed analog application. First, the MOS FETs have very low drive capability (they must even face large environment parasitics); Second, as shown in Fig.1b, large voltage headroom is necessary to ensure high-performance due to the large threshold voltage; Third, the realizable high-frequency performance relies strongly on the minimization of parasitic elements by layout optimization due to the larger poly-silicon gate resistance; Fourth, the lack of high-performance passive components due to the digital-circuit-aimed process.

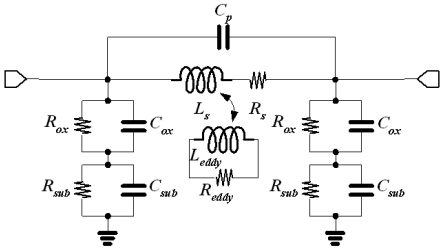
III. On-Chip Spiral Inductor

Motivation of inductor comes from the low-noise requirements of VCOs and the requirements of the matching and compensation techniques. The key points for designing the inductors are: 1) quality factor, 2) self-resonance frequency and 3) silicon area occupation.

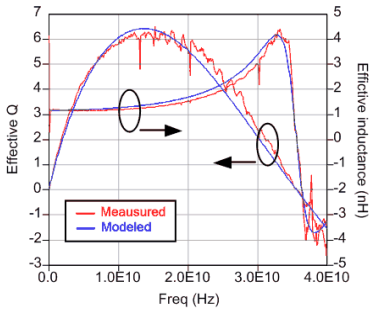
In standard digital CMOS technology the on-chip inductor suffers from three main parasitic effects which degrade its performance: 1) Ohmic resistance of aluminium thin-film causes loss, accompanied by high-frequency losses due to skin effect and eddy current effects in the conductor; 2) eddy currents in the heavily doped substrate cause a large degradation in the overall quality factor and reduce the inductance value; 3) parasitic capacitance to the substrate causes the inductor to be unusable above a certain frequency.

The planar spiral inductor has higher Q than solenoid, better controllability than bond wire, and is in addition more compatible with the IC interconnection scheme. Thus it is chosen for the design and optimization.

Inductors with different trace widths, trace spacing and hollow sizes have been simulated with the electromagnetic (EM) field analysis tool Momentum® and compared to study the influences of various geometrical parameters.



(a)



(b)

Fig. 2. Equivalent model of on-chip spiral inductor (a) and comparison of simulation with measured data (b)

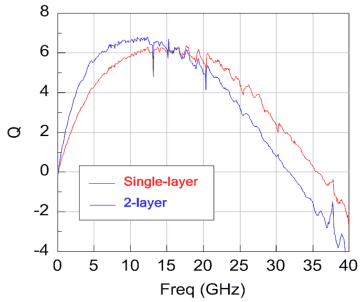
For the purpose of circuit simulation and Q optimization an appropriate lumped equivalent model for the interesting frequency range based on [1] has been adopted (Fig.2a). The constant parameters R_s *(Ohmic loss of metal)* and R_{eddy} *(magnetic loss in the substrate)* have been modified to be frequency dependent. A good match has been obtained between simulation of model and measured data up to 40 GHz (Fig.2b).

According to the relationships between the model parameters extracted from the EM simulation and geometrical parameters, a geometrical parameterized model is then used for Q optimization.

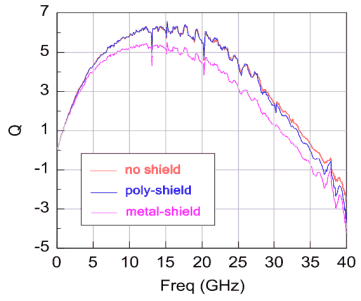
Besides the optimizations of latter structure, alternative techniques have also been investigated. i) The parallel metal layer inductor. ii) The inductor with widely used patterned ground shield (PGS) technique.

The parallel metal layer inductor shows a slight Q improvement without serious degradation of other performances (Fig.3a).

The widely used PGS technique, which can obviously reduce the Ohmic loss in lightly doped (in order of 10 Ω·cm) substrate, does not show much advantage in heavily doped substrate (as can be seen from the measured results in Fig.3b). Because for heavily doped substrate the main loss caused by magnetically induced eddy current cannot be prohibited by PGS. For metal ground shield, the reduced distance between the shield and the inductor trace even incurs the decrease of effective Q.



(a) Multi-layer trace



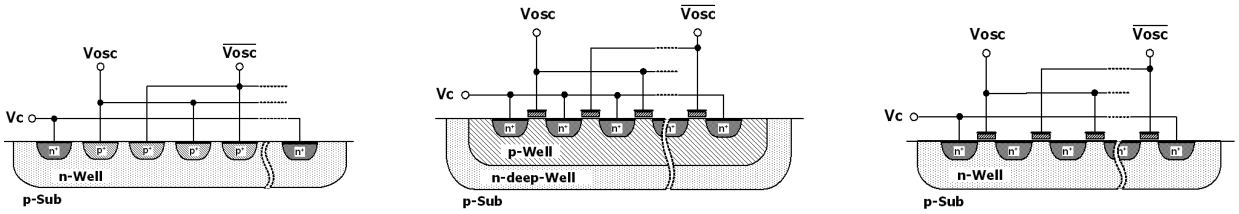
(b) Ground shield

Fig. 3. Alternative inductor techniques

An inductor with two-layer interlace structure has also been developed [2]. This structure presents smaller area occupation than normal ones without Q value degradation ($\sim 6.1 @ 10\,GHz$). It is adopted in the VCO design (Sec.V, Fig.5a).

IV. Varactor

As the passive inductor is given, the voltage-controlled capacitor (varactor) is needed for the VCO. The goals for the varactor design can be concluded as follows: 1) high quality



(a) The pn-junction varactor (b) Inversion mode varactor (c) Accumulation mode varactor

Fig. 4. Varactors with parallel and balanced configurations (a-c)

factor, 2) a large control voltage range compatible with the supply voltage, 3) good linearity over the available control voltage range, 4) a small silicon area.

In CMOS technology the varactor suffers from three main parasitic effects that degrade its performance: 1) the Ohmic losses in the substrate and the well and 2) the Ohmic losses of metal and poly-silicon interconnections, 3) the parasitic capacitances.

Three kinds of high-Q expected varactors, namely *pn-junction* varactor, *inversion-mode* nMOS varactor and *accumulation-mode* nMOS varactor with electrons as majority carriers have been designed and optimized [2] in parallel and balanced configurations [3] for differential application (Fig.4).

	Q (*min - max*)	C_{max}/C_{min}	Area eff. $(fF/\mu m^2)$	Bias lim.
inv-MOS	$23-36$	1.83	0.50	-
acc-MOS	$18-29$	1.70	0.50	-
pn-Junc.	$21-56$	1.62	0.16	$V_{pn}<0.6$

TABLE I
MEASURED RESULTS OF THE VARACTORS

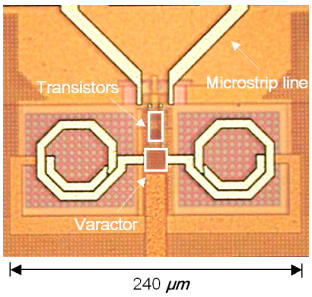
The measured results have been compared in Table. I. The higher losses in MOS varactor compared to pn-junction varactor come partly from the Ohmic loss of poly-silicon gate and partly from the high series resistance of the lightly-doped-drain (LDD) near the source and drain regions. Nevertheless, the MOS varactors are much more area-efficient and show more shapely tuning characteristics.

V. VOLTAGE CONTROLLED OSCILLATOR

10 GHz cross-coupled negative resistance LC VCOs [4] with three varactor versions mentioned above and ring LC VCO with injection function for injection locking application [5] have been implemented in the 0.18-μm digital CMOS technology [2].

The values of the on-chip inductors, varactors and cross-coupled FET pairs are chosen in respect of oscillation condition and tuning range. In particular, the inductance was made as large as possible for lower power consumption while maintaining a suitable frequency tuning range.

Despite the heavily doped substrate, reasonable phase noise performances and relatively large tuning range from cross-coupled and injection ring LC VCOs have been obtained from all varactor versions by using optimized two-layer interlace inductor and with careful layout design. The measured phase noise and power consumption excluding the buffers for cross-coupled LC VCO and ring LC VCO are around -105 dBc/Hz@1MHz and 7.2 mW as well as -101 dBc/Hz@1MHz and 32.4 mW under 1.8 V power supply, respectively. The indistinguishable phase noise performance of the different varactor versions are due to the close Qs of the resonance tanks, which are dominated by that of on-chip inductors. Nevertheless, VCOs with the MOS varactors give better linearity in the whole tuning range.



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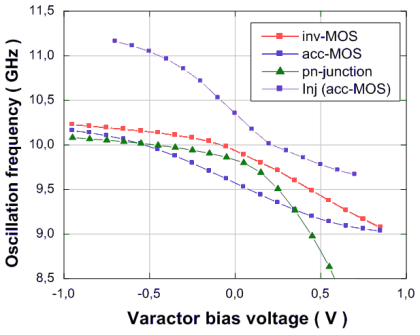


(b)

Fig. 5. LC VCO

Table. II is the results comparison with other published high-speed LC VCOs, which were fabricated on lightly doped non-epi substrate and hence could integrate on-chip inductors with higher Q. The VCOs in this paper show very close noise performance with them under the definition of FOM (*the figure of merit*) of oscillator given in [8], which includes the single

CMOS process	Substrate ($\Omega \cdot cm$)	Q_{ind}	Freq. (GHz)	Tuning (%)	Power con. (mW)	Phase noise (dBc/Hz)	FOM	Ref.
$0.25\,\mu m$	20	48	10	29.7	50	$-127@3MHz$	-180.4	[6]
$0.25\,\mu m$	15	-	17	8.6	10.5	$-108@1MHz$	-182.4	[7]
$0.18\,\mu m$	10^{-2}	6	10	12	7.2	$-105@1MHz$	-176.4	This work

TABLE II

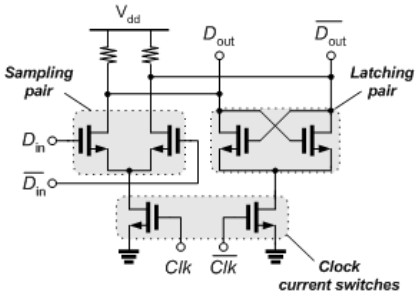
COMPARED WITH OTHER PUBLISHED HIGH-SPEED SINGLE-STAGE LC VCOS

side-band phase noise to carrier ratio S_{SSB} and the correction terms for carrier frequency f_0 and frequency offset Δf as well as power consumption P_{con}.

For the injection ring VCO, a locking range of 750 MHz with -4 dBm single-ended injection and 300 MHz with -10 dBm single-ended injection has been obtained.

VI. DATA DECISION CIRCUIT AND FREQUENCY DIVIDER

Considering the critical voltage allotment of the traditional stacked SCFL flip-flop structure under low supply, a kind of pseudo-differential structure has been investigated. By removing the current source, one less transistor level shares the supply voltage (Fig.6). This allays the problem of the allotment of the low supply voltage and hence improves the performance of transistors.



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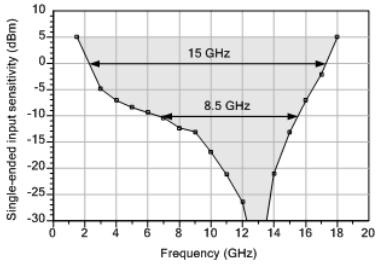

(b)

Fig. 6. Pseudo-differential latch and measured sensitivity of the frequency divider

The pseudo-differential D-type flip-flop based data decision circuit and the static frequency divider, which can operate up to 12.4 Gb/s and 18 GHz respectively, have been realized [9]. They serve also as performance indicators for other D-flip-flop based circuits such as multiplexers, demultiplexers and phase frequency detectors.

VII. DATA DECISION WITH FEEDBACK LOOP

As is well-known that decision feedback equalizers (DFE) can effectively mitigate inter-symbol interferences (ISI) in transmission channel [10].

A new DFE concept for a high-speed data decision with a feedback loop (DFL) for cancellation of ISI is investigated [11], [12], [13]. The improved speed performance has been obtained by a new concept merging the parallel principle [14] and a twin DC references approach [15].

The basic idea behind DFE is to subtract the ISI from a certain bit before the decision in the subsequent block. The ISI, in turn, is estimated based on the knowledge about the decision of the predecessor bit. In a straightforward manner, this principle can be implemented by feeding back the predecessor bit with a certain weight and subtracting this signal from the successor bit before its decision. The speed performance of this concept is, however, limited by the finite propagation delay of the feedback loop. To overcome this drawback, the combination of the use of two decision references, which correspond to the feedback signals for a preceded "0" and "1", respectively, and parallel approach has been proposed.

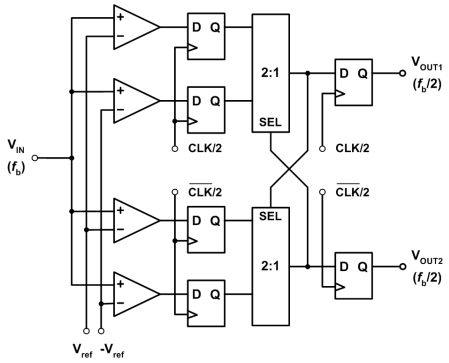

Fig. 7. Principle block diagram of DFL

Fig.7 shows the principle block diagram of the parallel data decision with feedback loop. Data, clock as well as references are complementary signals, but are drawn as single-phase signals for simplification. The circuit contains two parallel decision branches, which are triggered by rising edge and falling edge of $f/2$ clock, respectively.

Two comparators with complementary DC references V_{ref} and $-V_{ref}$ are in front of each branch. V_{ref} corresponds to a predecessor bit '1' while $-V_{ref}$ corresponds to "0". The current bit is decided in respect of both references simultaneously and latched in parallel paths. In fact, complementary data

inputs are fed to a differential amplifier, which is accordingly tilted by the reference voltages applied to a second differential pair working on the same loads. It shall be emphasized that both decisions can be performed without waiting for the predecessor decision results. The references can be externally adjusted to the actual ISI. Finally a 2:1 selector according to the predecessor bit will select the decision result of one of the paths.

The DFL prototype chip has been realized with an enhancement-depletion AlGaAs/GaAs HEMT technology with 0.2-μm gate-length and an f_T of about 60 GHz. The ISI cancellation function has been demonstrated in [12] and a maximum operating speed up to over 20 Gbit/s has been measured [13].

Presently, the concept is being migrated into CMOS technology with the optimized components.

VIII. Conclusion

The short-comings of the digital CMOS technology process can be overcome by the optimized device and circuit design techniques. The deep-submicron CMOS technology has the ability to offer a low-cost efficient integration of the analog high-speed ICs for the OC systems front-end.

Acknowledgment

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