Tunnelling Diodes for Compact Very High Speed Circuits

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The application of quantum tunnelling devices for high-performance digital circuitry is presented. The reliability of devices based on III/V semiconductor heterostructures is demonstrated and the applicability of emerging Si/SiGe heterostructures is discussed. The potential breakthrough of this approach is attributed to a very successful implementation in advanced circuit architectures. The applicability of Linear Threshold Gate logic based on the monostable–bistable transition logic element (MOBILE) is discussed here as the presently most promising candidate.

1. Introduction

The linear threshold logic is renewed as a strategy to extend the parallel processing capabilities on the gate level as an alternative to pure downscaling [1-2]. The success of this approach is strongly dependent on the availability of appropriate devices with a reliable I-V-characteristic with negative-differential resistance (NDR). This effect is provided by tunnelling devices (TD) such as interband- (ITD) [3] or resonant-tunnelling diodes (RTD) [4]. Today, among all quantum effect devices the tunnelling diodes are by far the most attractive candidates for high performance digital circuits competitive the mainstream of Silicon-based Boolean-Logic. This paper is organized as follows. In chapter 2 the tunnelling diode technology is sketched. The third chapter is dealing with the basic module, the MOBILE, and finally with its implementation in full-adder logic circuitry.

2. Tunnelling Diode Technology

2.1 III/V technology

Since the first realization of III/V RTDs in 1974 [4] a lot of materials aiming at higher conduction band discontinuities and better doping capabilities have been successfully investigated. This paper focuses on the promising InP-based technology. The layer stack for digital applications offering a medium peak current density of some 10^4 A/cm² and a low peak voltage (< 0.3 V) consists of two about 2 nm undoped AlAs barriers and an In(Ga)As well [5]. Previously, the manufacturability of RTD was a mayor concern because of the monolayer parameter sensitivity of the I-V-data. Today modern epitaxial growth equipment provides homogeneity on the wafer of typically less than 0.8 %. Consequently, the peak-voltage and peak-current homogeneity are in the order of 3 % and 5 %, respectively, while the reproducibility was within 7 % and 10 %, respectively. Hence, a full manufacturability of III/V based RTD can be stated.

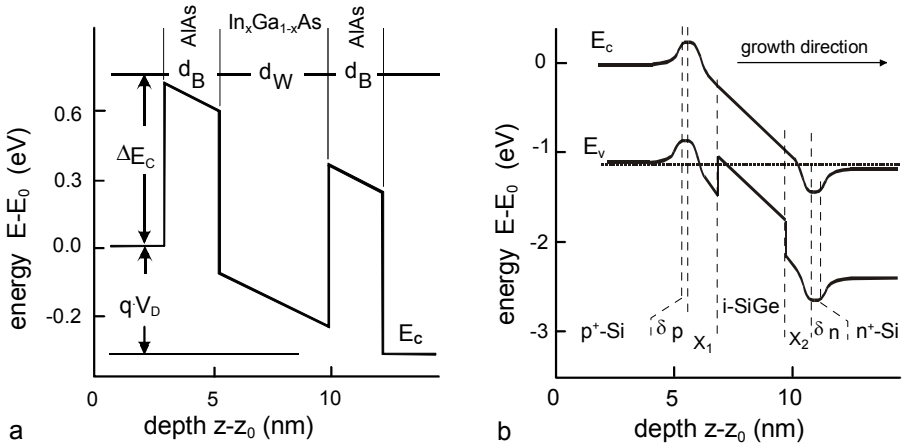


***Figure 1**. Energy band structure of Tunnelling Diodes:(a) InGaAs/AlAs double barrier RTD and (b) Si/SiGe TD.*

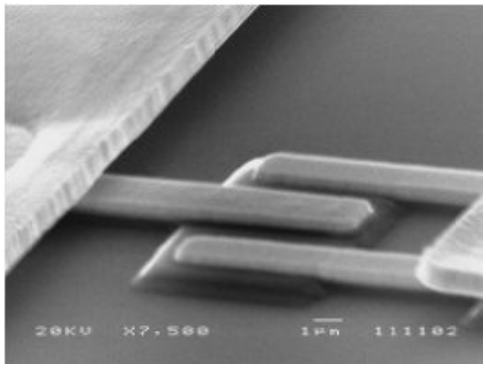
2.3 Si/SiGe technology

In order to hook-up to the silicon-mainstream of logic circuitry the development of any high-performance TD on the Si-substrate is highly attractive. The challenge of Si/SiGe heterostructures for RTD application is to provide a high positive conduction band discontinuity forming the electronic barrier. Using a virtual $Si_{1-x}Ge_x$ substrate the band structure at the Si/SiGe hetero-interface is altered such that only light transverse effective mass electrons may tunnel [6]. In the interband tunnelling diode (ITD) [3] the band-gap corresponds to the barrier height, which makes this device type more robust, compared to the Si/SiGe RTD. Recently Si and Si/SiGe-ITD's have demonstrated a high PVCR at reasonable current densities [7-9].

The Si/SiGe based layer stacks of this study were grown by solid source molecular beam epitaxy (MBE) on a high resistivity p^--Si substrate [7]. The layer structure is given in Fig.1b. The fabrication of the planar 2-metal ITD (Fig.2a) is described in [9]. The I-V-characteristics depend on the n- and p-spacer thickness as given in Figure 2b. The current density decreases dramatically with the p-spacer thickness x_1. At x_1 = 1 nm and at x_2 = 1 nm a current density of up to 17,000 A/cm² was obtained [7, 9]. In any ITD device the vertical spacing of highly doped layers is very narrow compared to RTD devices. The high capacitive load results in lower speed of the devices. The speed-index S_I defines the switching speed in the negative-differential region. The intrinsic ITD capacitance is (de-)charged by the ITD current from peak-current I_P to valley current I_V.

$$(V_P - V_V)\cdot C = (I_P - I_V)\cdot \Delta t \Rightarrow \frac{\Delta t}{\Delta V} = \frac{C}{(I_P - I_V)} = S_I \qquad (1)$$

For modelling the ITD the small-signal equivalent circuit given in fig. 2b is used. The parasitic environment is specified by the small-signal elements R_{ex}, L_{ex} and $C_{ex.}$ The use of silicon-substrate is accommodated by the RC-combination using the elements R_p and C_P. For modelling the intrinsic part of the ITD a combination of a resistance R and a capacitance C is necessary, in case of the NDR-region the resistance becomes negative. All devices of sample S1408 exhibit a speed index of 1 ns for 1 V of output voltage swing or better.



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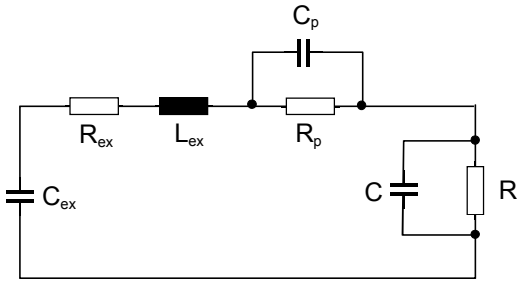

b

Figure 2. *Studied Si/SiGe ITDs: SEM micrograph of the 2-metal diode* (a) and small circuit equivalent circuits (b).

Tab. 1: Calculation of the speed-index for sample S1408 with different emitter area.

Emitter area	Peak-Current I_p	Valley-Current I_V	Capacitance C_P	Speed-Index S_I
10 µm²	1.56 mA	0.673 mA	570 fF	0.64 ns/V
20 µm²	3.36 mA	1.82 mA	1430 fF	0.93 ns/V
30 µm²	4.03 mA	2.23 mA	1800 fF	1.0 ns/V

3 MOBILE based Logic Circuit

The development of a fault-tolerant basic logic module is indispensable for a robust digital system. Among novel circuit architectures providing an optimum fault-tolerance the monostable-bistable-logic-element (MOBILE [10]) is the most promising approach for large scale tunnelling device circuits. The MOBILE is a clocked logic gate, which consists of two series connected TD. The MOBILE circuits are in a static, self-stabilizing state due to the inherent bi-stability of the TD. The MOBILE concept is very attractive for Linear Threshold Gate (LTG) Logic [1]. A LTG is a multiple input device that calculates the weighted sum χ of N inputs X_i. The weights w_i correspond to the TD area A_i in fig. 3a. The weighted sum is converted into a digital output Y by comparing χ with a given threshold value Θ:

$$Y\left(\vec{X}\right)=\operatorname{sgn}\left(\sum_{i=1}^{n} w_i X_i-\Theta\right)=\begin{cases}1 \text{ if } \sum_{i=1}^{n} w_i X_i \geq \Theta \\ 0 \text{ if } \sum_{i=1}^{n} w_i X_i < \Theta\end{cases} \tag{2}$$

The LTG offers a logic scheme for parallel computation beyond Boolean logic and may reduce the number of devices and the logic depth (latency). A combination of several LTG may result in an efficient realization of complex circuit functions. Addition is the most frequently used operation in general-purpose and application-specific processors. A full adder of bit i may be realized by means of two LTG gates, only (cf. Fig. 3b) providing the following computation:

$$\begin{aligned} c_i(\chi) &= sign\left(a_i+b_i+c_{i-1}-\Theta_1\right), \\ s_i(\chi) &= sign\left(a_i+b_i+c_{i-1}+w(c_i)\cdot c_i-\Theta_2\right). \end{aligned} \tag{3}$$

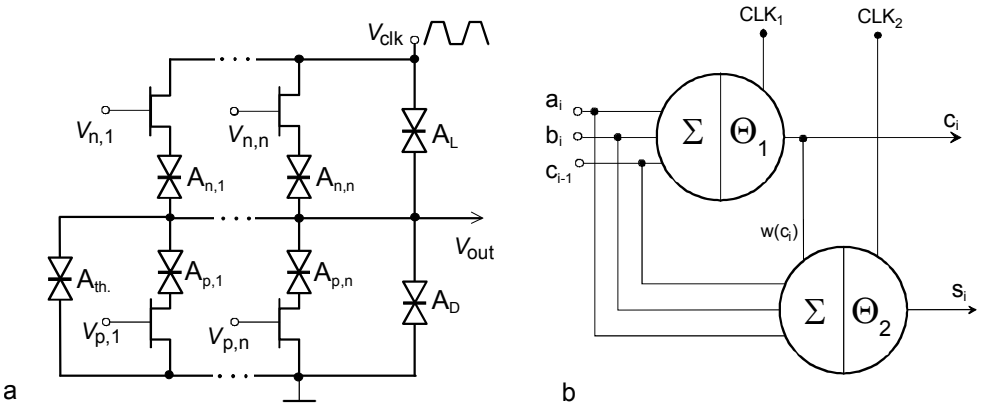

Figure 3. *Design of an advanced linear threshold gate with positive and negative weighted inputs using a FET/RTD combination as input terminal (b) and principal design of a full adder composed of two Linear Threshold Gates[2] .*

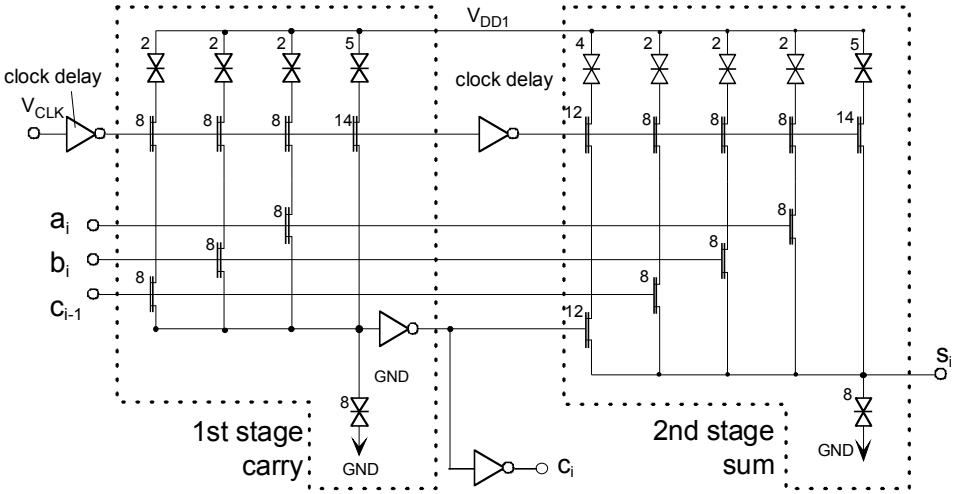

Figure 4. *1-bit depth-2 Full Adder: Principle of realization with Linear Threshold Gates (**a**) and schematics with local clock generation and time-shifted clock signals for the carrier and sum circuit [2]*

The 1-bit depth-2 threshold logic full adder demonstrator circuit is designed with MOBILE gates and RTD-HFET modules (Fig. 4). The transfer characteristic is obtained from a transient SPICE simulation to consider the charging of a 30 fF load capacitance and a clock slew rate of 1 V/ns. The performance data of a full adder with the RTD-HFET technology were simulated at a at a clocking speed 1 Gbit/s (cf. Table. 2). With reduced dimensions (0.1 µm minimum feature size) a clocking speed up to 5 GBit/s is expected.

Table 2. *Simulated performance and specifications of the full adder (V_{DD}=0.7V and f_{CLK} = 1 GHz)*

Value	data	data
level	high V_H=0.63 V	low V_L=0.08 V
power	$P_{average}$ = 725 µW	P_{max}=1.55 mW
rise-/ delay time	$t_r(c_i)$=250 ps, $t_d(c_i)$=144 ps,	$t_r(s_i)$=145 ps, $t_d(s_i)$=270 ps

4 Conclusions

The negative-differential resistance attributed to a voltage controlled tunnelling effect in quantum epitaxial heterostructures excited researchers in the past 3 decades. In the past decade Si-based tunnelling diodes emerged and the III/V tunnelling devices advanced to a high maturity. Present research is focusing on circuit development towards ultra-high speed digital operation and/or increased computational functionality. The MOBILE concept implemented in Linear Threshold Gate Logic is proposed here as a very attractive paths to further extend the performance of computational circuitry if the improvement of pure downscaling saturates in the silicon mainstream.

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