CMOS Wideband Amplifier with an Active Shunt Peaking Technique

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***Abstract*— Using an active shunt peaking technique to increase the bandwidth of the normal differential amplifier has been proposed. Based on this approach, the bandwidth of the CMOS differential amplifier could be improved by up to 80%.**

I. Introduction

The wideband amplifiers are one of the most critical building blocks in high-speed IC (Integrated Circuit). These amplifiers should have enough bandwidth and constant group-delay to avoid distortion in the wideband high-speed signals.

In spite of the continual performance improvement of the CMOS technology with its characteristic size scaling-down, the special compensation techniques are still necessary for the design of CMOS wideband amplifiers. Furthermore, the design with the down-scaled supply voltage and the inferior parasitic characteristics due to the conductive substrate in CMOS technologies faces more serious challenges.

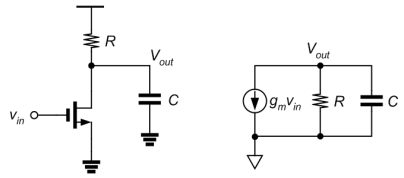
Many methods have been proposed in the past for the bandwidth enhancement: inductor shunt peaking technique [1], capacitive compensation technique [2], [3], [4], distributed amplification technique [5] and the active inductor technique [6].

This work introduces a parallel-connected active shunt peaking technique for designing CMOS low-voltage wideband amplifiers. This technique has all the advantages of other active inductor techniques and is suitable for low-voltage operation. No additional bias voltage like in [6] is necessary. The details of this technique and the simulated results of proposed CMOS differential amplifier in standard 0.18 μm technology are given in the following.

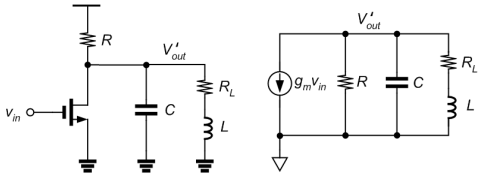
II. Circuit design

As mentioned above, CMOS circuits must also face the low supply voltage problem. The solution that replaces the passive inductor in [1] directly with the active one is not feasible due to the large drain-source voltage of MOS transistor in the saturation region. A parallel inductive compensation branch, however, shows the possibility for the realization of a low-voltage active shunt peaking.

We consider the simplified equivalent circuit of the common source amplifier shown in Fig. 1(a). Here, for simplicity, we assume that the small signal frequency response of the amplifier is determined only by the dominant pole at the output node.



(a) The common source amplifier and its equivalent model



(b) The common source amplifier with shunt peaking and its equivalent model

Fig. 1. Shunt peaking in a common source amplifier.

The voltage transfer function of the common source amplifier is given by

$$A_v(\omega) = \frac{v_{out}}{v_{in}} = -g_m \cdot \frac{R}{1 + j\omega RC} \tag{1}$$

where R and C are the output load resistance and the load capacitance, respectively.

Now we introduce an inductance L in series with a resistance R_L and add it parallel with the original *RC* load. The impedance of the inductive branch, increasing with the frequency, offsets partially the decreasing impedance of the *RC* network. It results a roughly constant gain over a broader frequency range and hence improves the bandwidth. We can also see from the transfer function of the compensated amplifier shown below. It has two poles and one zero. The additional zero contributed by the inductive branch helps the enhancement of the bandwidth.

$$\begin{aligned} A_v^{'}(\omega) &= \frac{v_{out}^{'}}{v_{in}} \\ &= -g_m \cdot \frac{R_L + j\omega L}{(1+R_L/R) + j\omega(L/R + R_L C) - \omega^2 LC} \end{aligned} \tag{2}$$

It should be noted that, R_L should be in an appropriate range for getting an enhanced low-pass characteristic. With the parallel shunt peaking, the dc gain is reduced from $A_v(0) = -g_m \cdot R$ to $A_v^{'}(0) = -g_m \cdot R_{dc} \cdot (R//R_L)$.

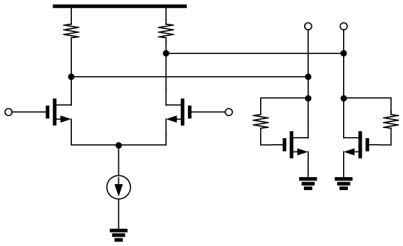
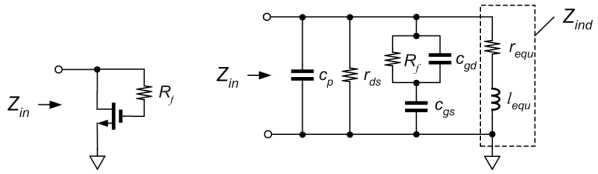


Fig. 2. Proposed CMOS active shunt peaking wideband differential amplifier

Fig. 2 shows the schematic of the CMOS wideband differential amplifier with the active shunt peaking. The inductive branch is composed of an n-type MOS transistor operating in the saturation region and a resistor. Its equivalent model is shown in Fig. 3.



(a) (b)

Fig. 3. The active inductive branch and its equivalent model

The equivalent input impedance is a parallel connection of the total parasitic capacitance C_p, the output resistance of the transistor r_{ds}, the *RC* network composed of $R_f C_{gd} C_{gs}$, and the required inductive impedance Z_{ind}, which is given by

$$Z_{ind} = \frac{1}{g_m} \cdot \left(1 + \frac{j\omega R_f C_{gs}}{1 + j\omega R_f C_{gd}}\right) \tag{3}$$

If we look insight into the operating mechanism, we can find that the voltage-controlled current source and a *RC* network realize the function of an ideal inductor: when the voltage at the input node changes, the current of the source which is controlled by gate-source voltage will not follow the change immediately but is delayed due to the *RC* low-pass network between the input node and the gate node.

For the purpose of the analysis and the design, we express the Z_{ind} as:

$$Z_{ind} = r_{equ}(\omega) + j\omega l_{equ}(\omega) \tag{4}$$

where

$$\begin{aligned} r_{equ} &= real(Z_{ind}) \\ &= \frac{1}{g_m} \cdot \left(1 + \frac{\omega^2 R_f^2 C_{gs} C_{gd}}{1+\omega^2 R_f^2 C_{gd}^2}\right)\Big|_{R_f \ll \frac{1}{\omega C_{gd}}} \\ &\approx \frac{1}{g_m} \end{aligned} \tag{5}$$

$$\begin{aligned} l_{equ} &= \frac{imag(Z_{ind})}{\omega} \\ &= \frac{R_f C_{gs}}{g_m\left(1+\omega^2 R_f^2 C_{gd}^2\right)}\Big|_{R_f \ll \frac{1}{\omega C_{gd}}} \\ &\approx \frac{R_f C_{gs}}{g_m} \end{aligned} \tag{6}$$

So the quality factor *Q* of Z_{ind} is given by

$$Q = \frac{\omega l_{equ}}{r_{equ}} \approx \omega R_f C_{gs} \tag{7}$$

Note that when the condition $R_f \ll 1/(\omega C_{gd})$ is fulfilled in the interesting frequency range, the effect of C_{gd} can be ignored, r_{equ} and l_{equ} are almost frequency independent. This gives a rough guidance of the component parameters and simplifies the design.

Except the wanted inductive component, the sub-circuit induces also unwanted parasitics. As it can be seen in Fig. 3(c), C_p that includes parasitic capacitances from both the transistor and the resistor should be minimized. (The resistor-induced partial parasitic capacitance appearing at the gate node will be added on C_{gs}.) The transistor output resistance r_{ds} is normally larger than the load resistance and has little influence on the gain. Because the condition $|1/j\omega C_p| \ll |R_f + 1/j\omega C_{gs}|$ is usually fulfilled, the self-resonance frequency of the active inductor can be deduced from

$$f_{self-res} \approx \frac{1}{2\pi\sqrt{l_{equ} C_p}} \tag{8}$$

By applying the expression (6) of l_{equ}, we have

$$f_{self-res} \approx \frac{1}{2\pi} \cdot \sqrt{\frac{1}{\frac{R_f C_{gs} C_p}{g_m} - R_f^2 C_{gd}^2}} \tag{9}$$

In practice, fortunately, these parasitics haven't brought much trouble to baffle the application. The optimized active inductor for 10 Gb/s data buffer with an inductance of about 8 nH shows a self-resonance frequency of about 15.5 GHz which is much larger than the –3 dB frequency.

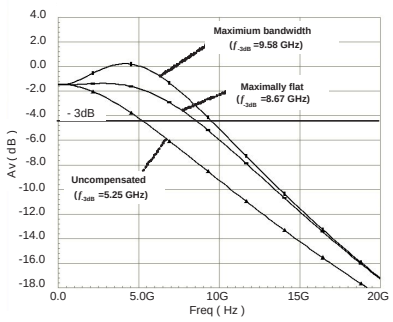
The pMOS counterpart of active inductor has lower g_m and hence lower self-resonance frequency.

III. Simulation

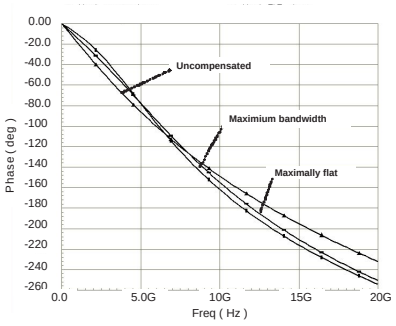
The active shunt peaking technique has been verified by designing a CMOS wideband buffer for 10 Gb/s data. Its task is to buffer the data signal and drive the external 50 Ω terminal. The whole buffer is composed of three compensated differential gain stages and one interface stage. The gate width of the amplification transistors in the first gain stage is 10 μm so that it can be driven by the small core function circuit.

The buffer is built in a standard digital 0.18 μm CMOS technology. The simulation was performed with Spectre® simulator excluding only the interconnection parasitics. The simulated small-signal frequency responses are shown in Fig. 4. In order to compare the performance, the result of a normal differential amplifiers based buffer, which has identical bias and dc gain with compensated amplifiers, is shown together.

The simulated bandwidth of the maximum-bandwidth-optimized buffer is about 9.58 GHz. And that of the maximally-flat-optimized buffer is about 8.67 GHz. Compared to the bandwidth of the normal buffer 5.20 GHz; both have



(a)



(b)

Fig. 4. Simulated gain-frequency and phase-frequency responses of the buffer amplifiers

evident bandwidth enhancements (about 80% and 65% respectively).

Fig. 5 shows the simulated single-ended transient waveforms and the eye diagrams at 10 Gb/s. All three buffers draw same 27 mA current from 1.8 V power supply.

IV. Conclusion

An active shunt peaking technique has been developed to increase the bandwidth of the differential amplifier. The bandwidth of the proposed CMOS differential amplifier is 80% higher compared to the normal one. This approach requires very small additional chip area and is compatible with low supply voltage.

Acknowledgment

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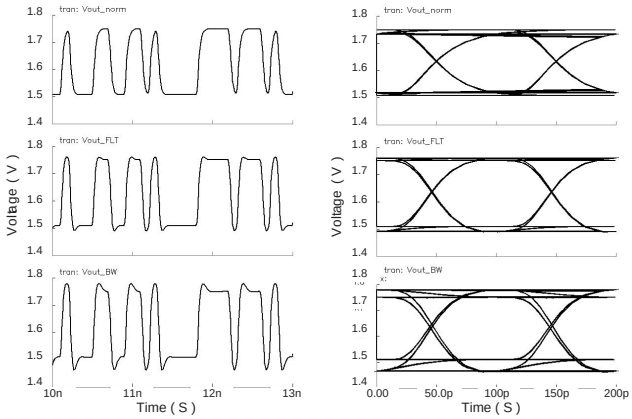

Fig. 5. Simulated single-ended output waveforms and eye diagrams of the buffer amplifiers with 10 Gb/s input
From top to bottom: (a) The uncompensated amplifier; (b) The maximally flat compensated amplifier; (c) The maximum bandwidth compensated amplifier

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