# SiGe Bipolar ICs for 40 Gb/s Fiber-Optic TDM Transmission Systems

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## 1. Introduction and System Concept

Today, commercial time-division multiplexing (TDM) systems for long-haul optical-fiber links are running at 2.5 and 10 Gb/s, respectively. Based on these systems the transmitted data rate is further increased by wavelength-division multiplexing (WDM). To meet the increasing demand on transmission capacity for future optical-fiber links, TDM systems with data rates as high as 40 Gb/s are under development. For Si-based technologies it was recently demonstrated, that all ICs required in a TDM link running at 40 Gb/s can be realized in an advanced SiGe technology [1] (in this reference also all the other references concerning this paper are listed).

In order to achieve 40 Gb/s even with the speed-critical circuits, the TDM system in Fig. 1 is used. It allows relaxed specifications for the ICs compared to conventional 10 and 20 Gb/s systems and is similar to the one applied by Siemens in a 40 Gb/s TDM system (see German R&D program Photonik II). In the transmitter, the last stage of the 4:1 time division multiplexer (MUX) is replaced by a power version of this circuit ("power MUX"). It stands out for steeper pulse edges and smaller time jitter compared to a conventional modulator driver. These advantages are a consequence of the clocked operation and the inherent retiming capability of the power MUX. However, for the design of both driver concepts a symmetrical configuration of the electroabsorption modulator (EAM) is assumed in order to halve the output voltage swing to be generated. (This assumption may no longer be required if EAMs for lower voltage swings (e.g. < 1.5 $V_{p-p}$) are available.) In the receiver, a gain-controlled optical amplifier (OA) is used in front of the photodiode (PD). This measure relaxes the demands on gain, dynamic range, and input sensitivity of the succeeding transimpedance amplifier (TIA). The decision function is performed by the first (1:2) stage of the 1:4 DEMUX (clock frequency 20 GHz) rather than by a single master-slave D-flip-flop (MS-D-FF), resulting in important advantages: A 1:2 DEMUX stands out for a higher operating speed at excellent retiming capability and a higher input sensitivity. Moreover, the clock frequency is halved to 20 GHz so that the clock recovery circuit is no longer a speed-critical component.

## 2. SiGe Bipolar Technology

All circuits were realized in a SiGe bipolar technology of Siemens (now Infineon). It is a self-aligned double-polysilicon technology with 0.5 µm lithography (resulting in an effective emitter stripe width of 0.3 µm) and three metallization layers. A gradient of the Ge concentration in the epitaxial base causes an accelerating drift field, which reduces the transit time $\tau_f$ and thus increases $f_T$ (≈72 GHz) and $f_{max}$ (≈74 GHz). The speed potential is further increased by the high admissible collector current density of $j_{CK} \approx 2$ mA/µm² (at $V_{CE}$=1 V). Typical parameters for a transistor with 10 µm emitter length are junction capacitances of $C_{EB}$=28 fF, $C_{CB}$=19 fF, and $C_{CS}$=20 fF (zero-bias values), base resistance of $r_B$=38 Ω, and transit time of $\tau_f$ =1.7 ps. It should be noted that during design and fabrication of the ICs, the technology used was in a laboratory state. However, in 2000 a production technology of Infineon (B7HF) with even better transistor parameters and 4-level metallization is available, which would further improve circuit performance.

## 3. Mounting and Measuring Techniques

Apart from the transimpedance amplifier and the power MUX for which $Al_2O_3$ ceramic substrates and an industrial measurement socket with low thermal resistance (only for power MUX) were used, all the ICs were mounted in a simple and inexpensive way, which proved to be suited for data rates up to 60 Gb/s. The measurement socket consists of a 254 µm thick teflon substrate (PTFE) with low permittivity ($\varepsilon_r$ = 2.2) which is soldered on a brass block. The chip is glued into a recess in this socket and then conventionally ultrasonic bonded. By this measure, the chip surface is about at the same level as the microstrip line, so that the bond-wire lengths and thus the bond inductances are reduced. A photograph of the complete measurement socket for the 60 Gb/s MUX is shown in Fig. 2. At the data inputs (30 Gb/s) and the clock input (30 GHz) K-connectors are used. To achieve a low reflection coefficient at the output (60 Gb/s), a semi-rigid cable, whose diameter fits the substrate thickness, was directly connected to the measurement socket by means of a simple fixture. Similarly good results were obtained with K-connectors in a slightly modified assembly compared to the manufacturer's instructions.

For measuring the developed ICs a pulse sequence generator with data rates up to 60 Gb/s is required. Since such a generator is not yet commercially available we built a quasi pseudo-random bit-pattern generator (PRBG) by using our own circuits. For this, the two independent outputs of two 7.5 Gb/s PRBGs are multiplexed up to 60 Gb/s.

## 4. Configuration and Measurement Results of the High-Speed ICs

All circuits were designed on the base of the SiGe bipolar technology mentioned above by consequently applying the circuit principles and design aspects described in [2].

**60 Gb/s MUX.** The circuit diagram of the MUX, shown in Fig. 3, is typical for high-speed digital circuits. It differs from the usual ECL, which is not suited for very-high-speed applications in a transmission line environment, by the following features: The output stage is a current switch (CS) configuration, while the data input buffers are multiple emitter followers (EF); differential operation with low voltage swing is used; the transmission lines are matched at the input and (partly) at the output by on-chip resistors. For the MUX core series gating of the data and clock signals is applied. A separate output buffer is not used, in order to obtain maximum operating speed. The MUX core was designed to switch 10 mA, resulting in a differential output voltage swing of 0.5 $V_{p-p}$ at 50-Ω on-chip matching and 50 Ω external load. The power consumption is 300 mW at a single supply voltage of -5 V.

Fig. 4 shows a section of the output pulse sequence (top) and the clear eye diagram (bottom) of the mounted MUX chip at an output data rate of 60 Gb/s. Part of the time jitter is caused by the measurement setup [1]. The rise and fall times (20 to 80%) of the pulse edges are about 7 ps, including the degradation caused by the limited bandwidth of the measurement setup and the sampling scope (HP 54124). The clock phase margin at 60 Gb/s is still 130°, demonstrating the retiming capability even at this high data rate. Although this MUX is not required in the proposed transmitter concept of Fig. 1, it is a useful device in very-high-speed applications, e.g. as the final stage of our bit-pattern generator used for measuring all the ICs presented in this paper.

**40 - 50 Gb/s Power MUX as a Modulator Driver.** In order to benefit from the inherent high speed capability of the MUX, a power version of the MUX was developed to drive the EAM directly. Its simplified block diagram is shown in Fig. 5a. Besides the much higher switched output current (up to 50 mA), the main differences compared to the 60 Gb/s MUX are as follows. At the (50-Ω) data inputs, more powerful buffer stages are used, which each consist of a current switch with two EF pairs at its input and three at its output. Compared to using only two or three EF pairs the input capacitance (in parallel to the 50-Ω on-chip resistors) is reduced and thus transmission line matching is improved. Moreover, much smaller signal amplitudes are required at the data inputs (≈ 300 $mV_{p-p}$). At the output of the MUX core, a (differential) grounded-base stage (GBS) is used, in order to mitigate the transistor breakdown problems and to increase the operating speed. At the output of the power MUX, a network for biasing the (symmetrical) EAM is connected in series to the load resistors $R_Q$ (= 25 Ω). The bias voltage $V_{Bias}$ can be varied between 0 V and -2 V via an external potentiometer, at a nominal value of -1 V. The total power consumption of the chip is 2 W.

For the measurements, the chip was mounted on a special socket with low thermal resistance. As confirmed by careful simulations, the signal across the EAM quantum wells agrees well with the output signal of the power MUX measured with an a.c. coupled 50 GHz sampling scope. For this, the on-chip resistances $R_Q$ must be increased from 25 Ω to 50 Ω (by scratching on-chip interconnections). As a consequence, the correct operation of the driver circuit can be verified by pure electrical measurements. Fig. 5b (top) shows the measured clear output eye diagram at the nominal data rate of 40 Gb/s with a differential voltage swing of 2.5 $V_{p-p}$. The clock phase margin at this data rate is 135°, confirming the important retiming capability of the circuit. Even at 50 Gb/s, sufficiently clear eye diagrams are obtained at the nominal swing of 2 $V_{p-p}$ (Fig. 5b, bottom), demonstrating the high speed potential of the power MUX. Both eye diagrams are given for the nominal EAM bias voltage $V_{Bias}$= -1V, but no degradation of signal performance was observed within the adjustable bias range of 0 to -2 V.

**40 Gb/s Transimpedance Amplifier.** To reduce costs and avoid critical interfaces, the amplifier was not separated into a pre- and a main amplifier; instead, the total circuit was realized on a single chip. Fig. 6a shows the block diagram of the transimpedance amplifier (TIA) with three basic amplifier cells. For all cells a fully differential configuration was chosen. Besides other advantages, this measure helps to reduce performance degradation caused by substrate coupling as well as by on-chip wiring and mounting parasitics. As shown by the simplified circuit diagram in Fig. 6b, each cell consists of a transimpedance (TIS) and a transadmittance stage (TAS), decoupled by three emitter-follower pairs (EF), and a grounded-base stage (GBS) at the output to mitigate potential transistor breakdown problems. Thus the principle of strong mismatching between succeeding transistor stages is consequently applied (cf. [1], [2]). At the output of the third cell (output stage), which must drive a (differential) 50-Ω transmission line, on-chip output resistors (60 Ω) are used to reduce double reflections.

Due to the high gain required, 40 Gb/s can hardly be achieved with completely linear operation. Therefore, only the first amplifier cell operates in the linear and the others in the limiting mode. As another advantage of limiting operation, the demanded constant output voltage swing is obtained without needing automatic gain control. In order to compensate the offset current which depends on the amplitude of the input current $i_I$, automatic offset control is applied, using a d.c. amplifier and a low-pass (LP) filter. As an option, an additional contribution to the input offset current can be adjusted for further minimizing the bit error rate of the receiver.

The amplifier chip (size: 0.9 mm × 1.4 mm) was mounted on a measuring socket applying $Al_2O_3$ ceramic substrate and K-connectors. In addition, for the pure electrical measurements a simplified PD model was realized on the substrate of the socket. The total PD capacitance is 65 fF. Fig. 6c shows the measured clear output eye diagram of the differential output voltage $v_Q$ at 40 Gb/s, for the lower limit of the input current swing, $\Delta I_I$ = 0.3 $mA_{p-p}$.(Even better signal quality at the same output voltage swing of $\Delta V_Q$ = 0.6 $V_{p-p}$ was observed at the upper specified limit of input current swing, $\Delta I_I$ = 0.6 $mA_{p-p}$.) Thus the maximum large-signal transimpedance in the limiting mode is $Z_{TI} = \Delta V_Q/\Delta I_I$ = 2 kΩ (while the small-signal transimpedance proved to be 10 kΩ). The total power consumption of the TIA is 800 mW at a single supply voltage of -6.5 V.

**60 Gb/s DEMUX.** Fig. 7 shows the block diagram of the 1:2 DEMUX which consists of the DEMUX core with two MS-D-FFs operating in parallel, the data and clock input stages, and two output buffers. The total power consumption of the DEMUX is 1.2 W at a single supply voltage of -5 V, including 0.6 W of the oversized high-speed 50 Ω output buffers taken from a modular concept.

The chip was mounted as described above and driven by a bit-pattern generator, with the 60 Gb/s MUX as the last stage, and by a 30 GHz clock. The measured eye diagram of the driving bit-pattern in Fig. 8a (top) is intentionally degraded in order to demonstrate the excellent retiming capability of the DEMUX even at 60 Gb/s. The output eye diagram in Fig. 8a (bottom) with a differential voltage swing of 640 $mV_{p-p}$ is well opened and shows only small time jitter. The clock phase margin (CPM) for this measurement is estimated to be about 180°.

Due to the intended application of the IC as a DEMUX with decision function in the receiver of a 40 Gb/s system, the CPM versus differential input voltage swing was measured at this data rate. The results in Fig. 8b demonstrate the high input sensitivity and excellent retiming capability of this circuit. This is of special interest since, to the best of the author's knowledge, single Si-based MS-D-FFs with such a high CPM and sensitivity at 40 Gb/s have not yet been reported. Therefore, for the decision function in the receiver of 40 Gb/s TDM systems the DEMUX should be preferred to the speed-critical MS-D-FF. Moreover, the DEMUX is part of the clock extraction circuit which generates 20 GHz from the 40 Gb/s data stream. For this, additionally a single MS-D-FF (clocked at 20 GHz), two 20 Gb/s EXORs, and a VCO are used (cf. [1]).

## 5. Conclusions

It has been demonstrated by careful measurements on mounted chips, that all speed-critical ICs in 40 Gb/s TDM systems can be realized in advanced SiGe bipolar production technologies. This statement, however, includes the modulator driver only if adequate 40 Gb/s electroabsorption modulators (with their low required voltage swing) are available. Today, in 40 Gb/s systems $LiNbO_3$ modulators are preferred, which need much higher voltage swings, e.g. 5 $V_{p-p}$. To the best of the author's knowledge, no SiGe modulator driver meeting this strong demand has been reported until today.


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### References


[1] H.-M. Rein: "Si and SiGe bipolar ICs for 10 to 40 Gb/s optical-fiber TDM links", International Journal of High Speed Electronics and Systems, Vol. 9 (1998), No. 2, pp. 347-383, Special Issue on High Speed Electronics and Systems for Lightwave Communications, as well as in "High-Speed Circuits for Lightwave Communications", edited by K. C. Wang, in "Selected Topics in Electronics and Systems", Vol. 13, edited by P. K. Tien, World Scientific Publishing, Singapore, 1999.

[2] H.-M. Rein and M. Möller: "Design considerations for very-high-speed Si-bipolar IC's operating up to 50 Gb/s", IEEE Journal of Solid-State Circuits, Vol. 31 (1996), pp. 1076-1090.


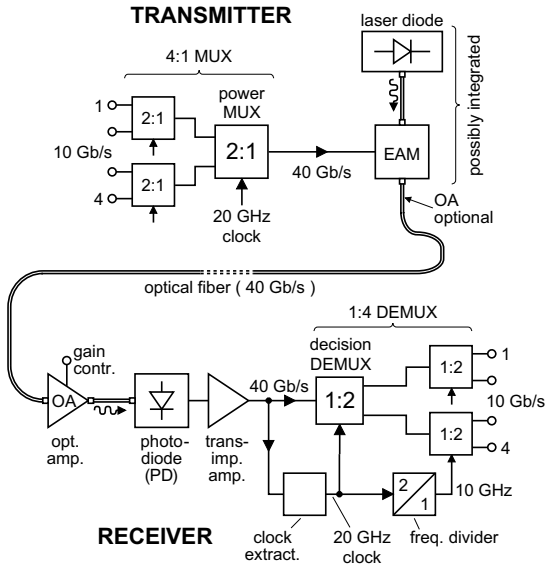


Fig. 1: Scheme of a 40 Gb/s optical-fiber TDM link, allowing relaxed circuit specifications.

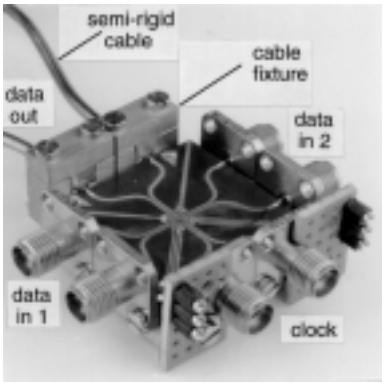


Fig. 2: Measurement socket of the 60 Gb/s MUX. Size of substrate is about 3 cm x 3 cm.

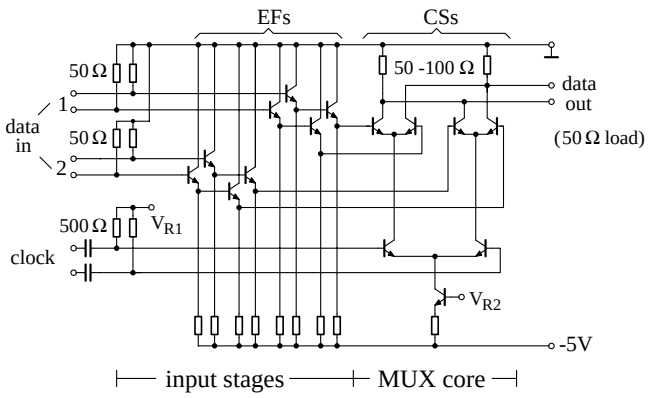


Fig. 3: Circuit diagram of a high-speed 2:1 MUX.

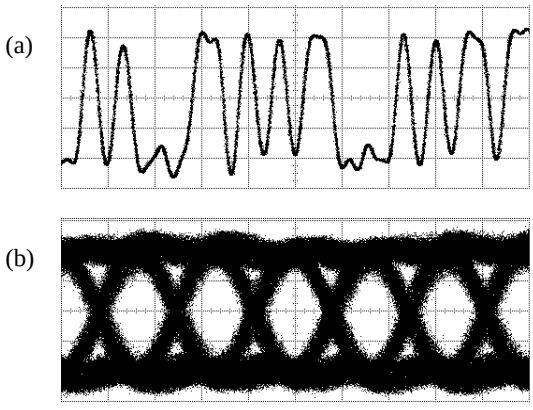


Fig. 4: Measurement results of the MUX at 60 Gb/s output data rate.
(a) Section of output pulse sequence (50 ps/div., 125 mV/div.).
(b) Output eye diagram (10 ps/div., 125 mV/div.).

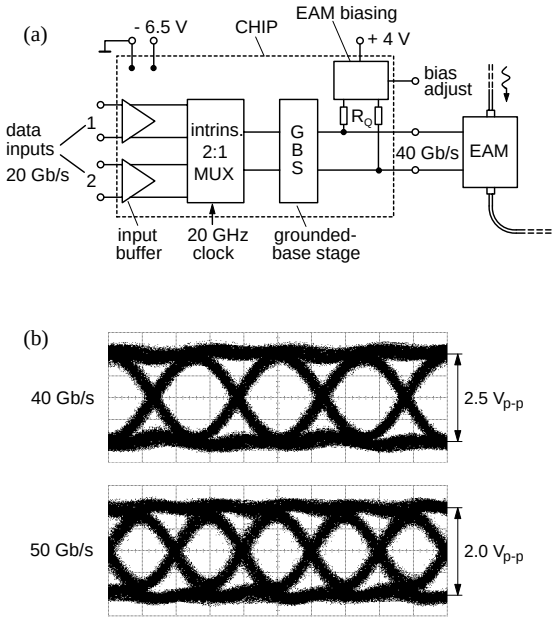


Fig. 5: Power MUX for driving the EAM in a 40 Gb/s link.
(a) Simplified block diagram.
(b) Output eye diagrams (10 ps/div.).

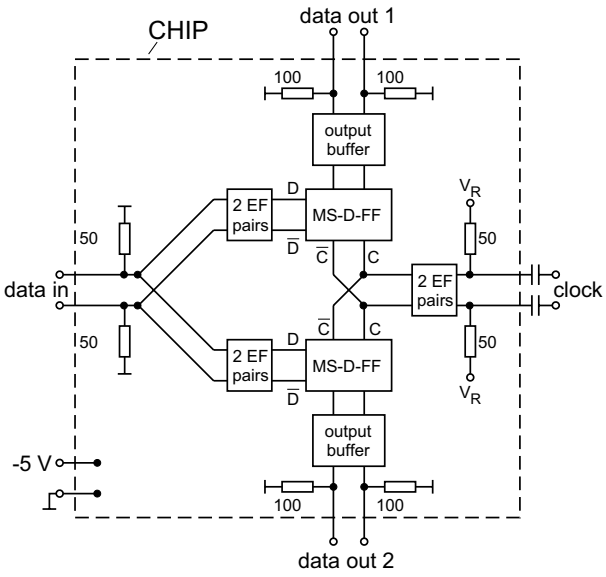


Fig. 7: Block diagram of a high-speed 1:2 DEMUX.

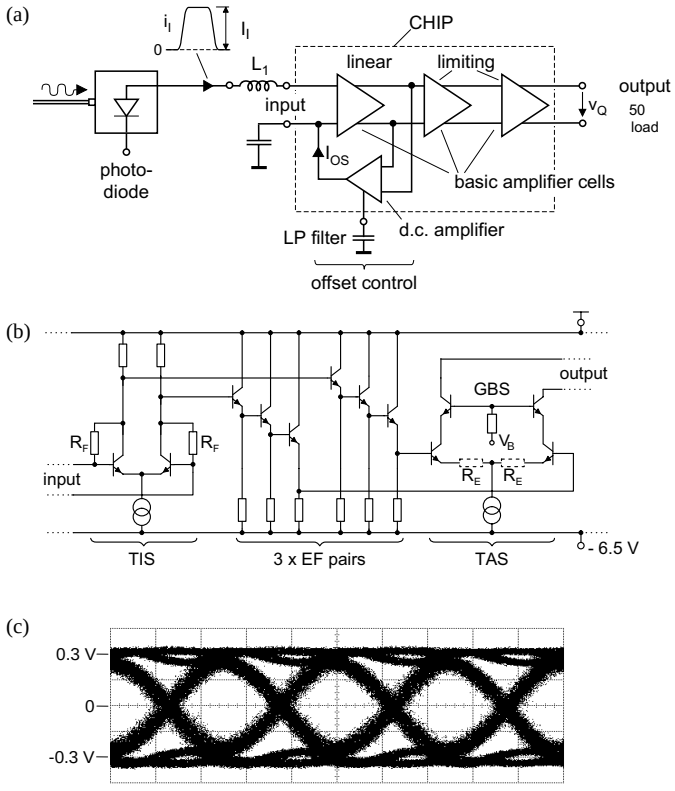


Fig. 6: Limiting transimpedance amplifier for a 40 Gb/s link.
(a) Simplified block diagram. (b) Basic amplifier cell.
(c) Output eye diagram at 40 Gb/s (10 ps/div.).

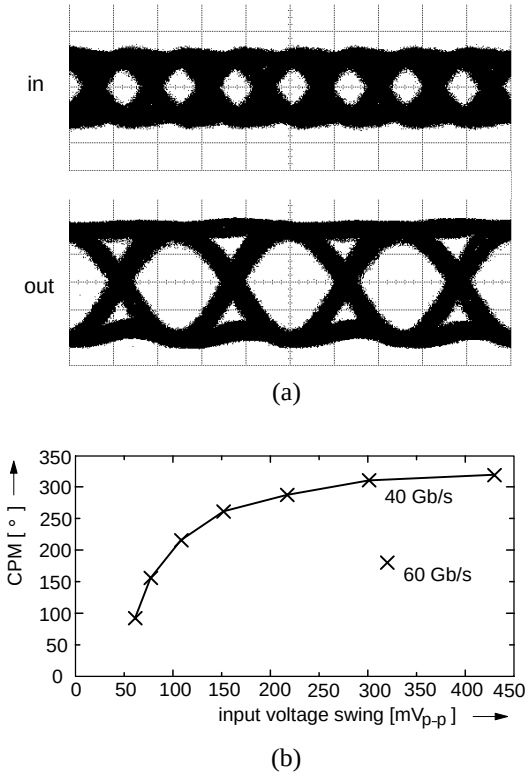


Fig. 8: Measurement results of the regenerating DEMUX.
(a) Eye diagrams at 60 Gb/s input data rate (160 mV/div., 13 ps/div.), CPM ≈ 180°.
(b) Signal regeneration capability at 40 Gb/s input data rate.