Trends and Challenges for ASSP and ASIC Design

Josef Sauerer
Fraunhofer Institut für Integrierte Schaltungen
Am Weichselgarten 3, 91058 Erlangen, Germany
www.iis.fhg.de

Abstract: *The Semiconductor Industrial Association (SIA) regularly updates its roadmap describing evolution of technologies and design methodologies for the next decade. This roadmap predicts chip complexity rising well beyond half a billion transistors per chip, clock frequencies going up to some GHz and supply voltages going down to around 1 V. Design methodology will have to change to increase design productivity and to scope with the timing and signal integrity problems related to deep submicron system-on-chip development.*

On the commercial side, mask costs will rise from around 50 k US$ for 0.5 um CMOS technology to well beyond 500 k US$ for 0.09 um CMOS. Wafer production will be economy-of-scale oriented based on increasing wafer diameters. Hence the development described in the SIA roadmap concerns mainly very high volume digital applications like data processing and public switched telephone network.

In many other applications, i.e. in the mixed signal, RF or high speed optics area, technology requirements and due to the lower production volumes we usually find there, also commercial constraints are quite different. This is especially true for the ASSP and ASIC domain. In order to make an ASSP or ASIC development successful, all the parameters influencing performance, development time, overall project costs and volume cost have to be evaluated carefully before selecting technology and design methodology.

Technology trends for ASIC and ASSP development: Since more than 30 years “Moore’s law” saying that chip complexity doubles every 18 months and cost-per-function decreases by about 30 % per year is a consistent macrotrend for semiconductor industry (Fig. 1). This trend is driven by CMOS technology development. Therefore CMOS has already taken the biggest share and will continue to increase it in ASIC and ASSP applications because it fully benefits from the progress made in the

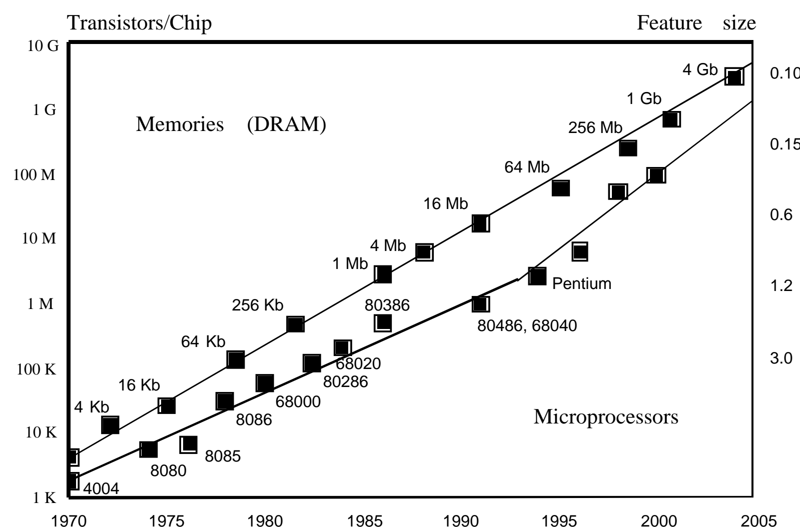


Fig. 1: Integration density and feature size for memories and logic

mainstream digital area in terms of integration density, performance, maturity for production and cost optimisation (Fig. 2). The integration density now available with CMOS allows to develop complete systems-on-a-chip including highly precise analogue blocks, RF front-ends, sensors or MEMS. Additional process-modules employing additional masks (Table 1) and resulting in higher costs are necessary to implement these features but at high volumes this cost penalty is compensated by

decreasing interconnect costs (Fig. 3) and improved functionality. But in future CMOS generations, more and more

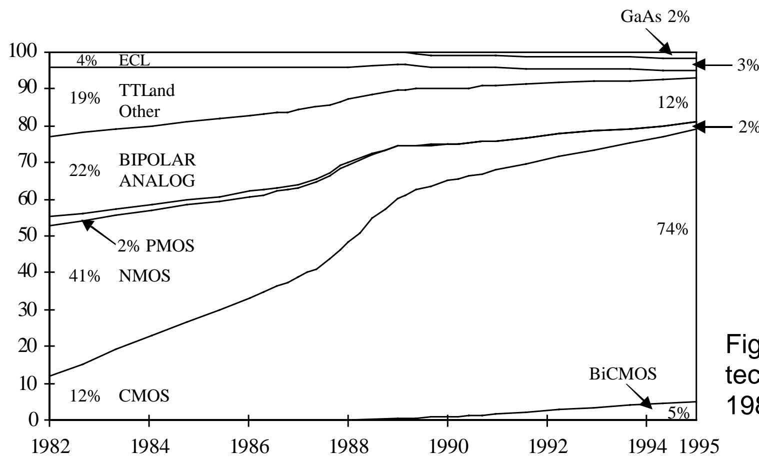


Fig: 2: Development of technology shares between 1982 and 1995

increasing mask levels for additional technology modules	Logic	SRAM	Flash	DRAM	CMOS RF	FPGA	MEMS	FRAM	Chemical Sensors	Electro Optical
Logic	0									
SRAM	1-2	0								
Flash	4	3-4	0							
DRAM	4-5	3-4	7-9	0						
CMOS RF	3-5	5-9	6-9	6-10	0					
FPGA	2	2-4	4-6	3-7	5-7	0				
MEMS	2-10	3-12	6-14	6-15	5-15	4-12	0			
FRAM	4-5	3-4	7-9	2-3	7-10	6-7	9-15	0		
Chemical Sensors	2-6	3-7	6-10	6-11	5-11	4-8	4-16	6-11	0	
Electro-Optical	5-8	6-9	9-12	9-13	8-12	7-10	7-18	9-13	7-14	0

Table 1: Increasing mask levels for additional technology modules

deep-submicron effects and the reduced supply voltages limiting signal swing for analogue circuits will result in using technologies some generations behind the leading edge. This trend is not only due to technical reasons but also due to increasing NRE costs: On the economical side, before the end of the decade we will face the fact that transition to latest generation technology is no longer commercially attractive for many applications especially in the ASSP and ASIC domain.

Nevertheless, bipolar technologies, still quite strong in the analogue area, more and more will loose market shares to CMOS or BiCMOS. BiCMOS technologies combining the advantages of CMOS with the higher speed and better driving capabilities of bipolar technologies at slightly higher costs will complement CMOS in the lower GHz range. By replacing the bipolar transistor by a SiGe HBT, BiCMOS technologies will extend into application areas currently covered by GaAs MESFET technologies.
GaAs technologies in the last couple of years have established in the market and will maintain a small but stable market share for high frequency applications not only as standard products but also in the

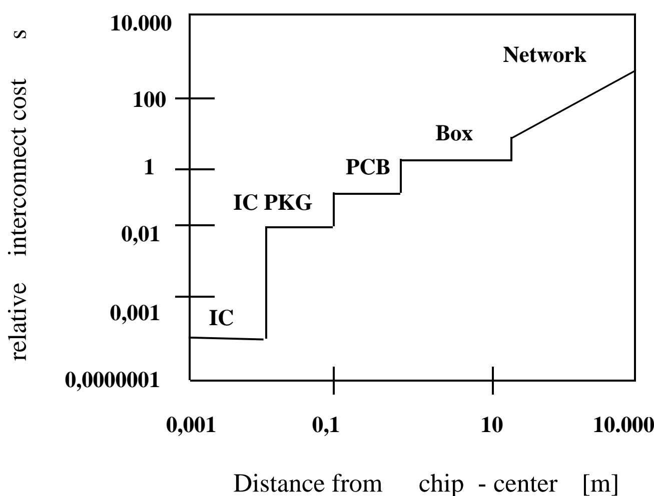
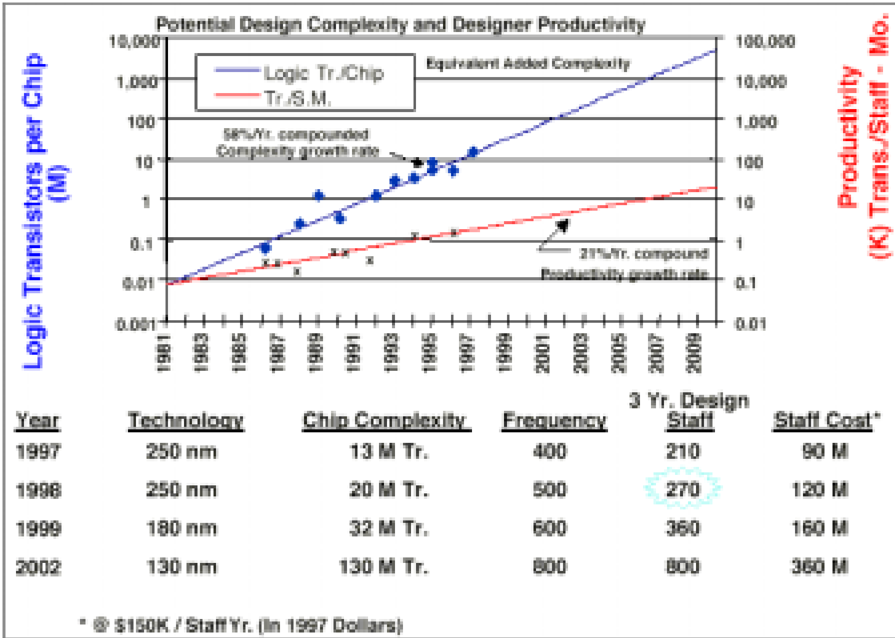


Fig. 3: Relative interconnect costs as function from distance from chip center

ASIC domain. InP technologies have demo nstrated their capabilities i.e. for high speed optics but extremely high costs and still low maturity prevent them from being frequently used in industrial ASIC projects.

Facing rapidly increasing NRE-costs for advanced technologies on the one hand and steadily increasing wafer diameters combined with decreasing feature sizes resulting in more and more dies per batch on the other hand it will be more and more difficult to get prototypes and small volumes necessary for niche application. Multi-Project-Wafer (MPW)-Services set up in the US and Europe in the late 80s will play an important role in future microelectronics to serve these markets. In Europe, EUROPRACTICE, a EU-funded MPW service, already serves dozens of industrial customers with low cost prototypes and small volume production.

Design challenges: Maximum integration density is growing with more than 60 % per year but design productivity only has an average growth rate of 21 % per year. This means there is a growing productivity gap which becomes even worse because of generally decreasing time-to-market (Fig. 4). The transition to semicustom design methodologies employing automatic Place-and-Route and logic



Year	Technology	Chip Complexity	Frequency	3 Yr. Design Staff	Staff Cost*
1997	250 nm	13 M Tr.	400	210	90 M
1998	250 nm	20 M Tr.	500	270	120 M
1999	180 nm	32 M Tr.	600	360	160 M
2002	130 nm	130 M Tr.	800	800	360 M

* @ $150K / Staff Yr. (In 1997 Dollars)

Fig. 4: The design productivity gap [1]

synthesis during the 80s and early 90s brought some help. But with the transition to system-level-integration (SLI) based on deep submicron technologies we are experiencing today new design challenges coming about:

First the classic ASIC platform consisting of process technology and standard cell ASIC library has to be extended versus an SLI platform by including (third party) IPs like processor cores and digital macros like memories as well as analogue blocks like Analogue-to-Digital converters. More and more products will be software defined, hence embedded software and methodologies for hardware/software codesign become important. Application specific know-how has to become an integral part of the IC development team (Fig. 5). Design houses and semiconductor companies which were Silicon suppliers for decades now have to enter strategic alliances with system partners and become (sub)system suppliers.
Second, when proceeding to deep submicron (DSM) technologies understanding process impact on design and hence the verification issue becomes more and more important. Whereas all the way down to the 0.8 um mainly area and speed were the critical parameters which had to be checked during the design process. Power dissipation and self heating became critical in the 0.7 um and 0.5 um process generations. Now signal integrity, EMI and metal migration aspects have to be taken into account.

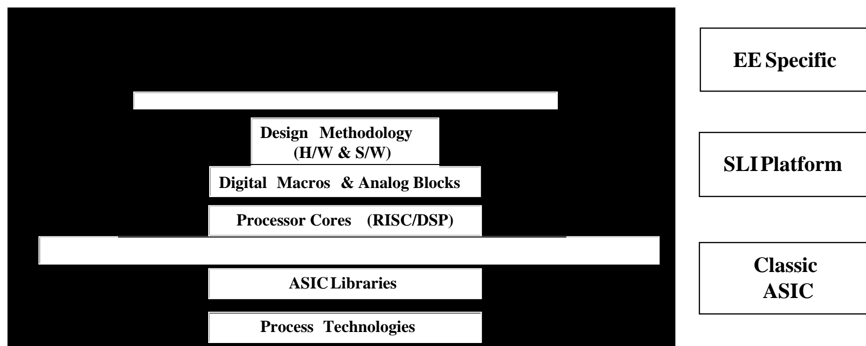


Fig. 5: Capabilities needed for system-level-integration were accustomed to supply customers with Silicon

Especially when including 3rd party IPs design verification and testing strategies become major issues (Table 2). As soon as RF front ends or sensors are included in the integrated systems standard

	0,8 µm	0,7 µm	0,5 µm	0,35 µm	0,25 µm	0,18 µm
area	✓	✓	✓	✓	✓	✓
speed	✓	✓	✓	✓	✓	✓
power dissipation		✓	✓	✓	✓	✓
metal migration				✓	✓	✓
CMP					✓	✓
signal integrity					✓	✓
test concept					✓	✓
EMI						✓
encapsulation						✓

Table 2: Critical parameters influencing design success for different technology generations

encapsulation can not longer be used and package development has to become part of the project. High level design and design automation tools were considered as way to higher design productivity during the 90's. But with the interrelations between system or application specific aspects and increased process impact on design we see now that for system level integration based on DSM technologies this approach is no longer viable facing the costs and time which is related with design iterations. Advances in design system architecture, design methodology and IP reuse will only cover part of the gap. Rather "...semiconductor industry will need to hire more and more circuit and system designers, software engineers, process technologists and skilled operators. Finding and training these key people may well become the industry's greatest problem, over and above the technological and financial challenges, and it may even become the major limiting factor to the growth in the next few years"[4].

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