# An Improved Decision Feedback Loop for Optical Communications

Li Wang, Zheng Gu, Andreas Thiede
Dept. of High-Frequency Electronics
University of Paderborn, Warburger Str. 100
33098 Paderborn, Germany
Phone: +49 5251 60 3388, Fax: +49 5251 60 4226
Email: liwang@hrz.uni-paderborn.de

Gang Wang, Rolf Kraemer
IHP GmbH, Technologie Park 25
15236, Frankfurt(Oder), Germany
Lothar Moeller
Lucent Technologies, 791 Holmdel-Keyport RD
Homdel, NJ 07733-400, United States

***Abstract*— Based on the structure proposed in [1] and [2], two new types of parallel decision feedback loops are presented. Efforts are made to secure the data transition and relax the delay limitation for the inner components. Additionally, the characteristics of four decision feedback loops are compared.**

## I. Introduction

In high-speed optical communications, polarization mode dispersion (PMD), chromatic dispersion or nonlinear pulse propagation and insufficient receiver bandwidth result in inter-symbol interference (ISI) in the received signal. ISI occurs as pre-cursor and post-cursor distortions. To mitigate the latter, various decision feedback equalizers (DFEs) have been investigated.

The first DFE for ISI mitigation in optical receivers which was introduced by Winters and Gitlin operated at 1.7 Gbit/s data rate [3]. A DFE targeted for 10 Gbit/s data processing was realized in [4], where the structure shown in Fig. 1 was adopted. However, the speed performance of this concept is limited by the delay of generating analog threshold in the feedback loop. To ease this limitation, two DC references, corresponding to the post-cursor interference imposed by the preceding signal "1" or "0", can be used as two decision thresholds [5]; this parallel look-ahead computation has been demonstrated in [1] and [2] by using AlGaAs/GaAs HEMT.

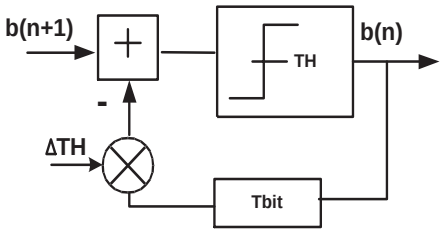


Fig. 1. DFE block diagram

## II. Existing structures of DFE

The basic principle of the DFE can be understood from Fig. 1. By feeding back the predecessor bit and subtracting the certain offset corresponding to it, the post-cursor of the predecessor bit can be overcome.

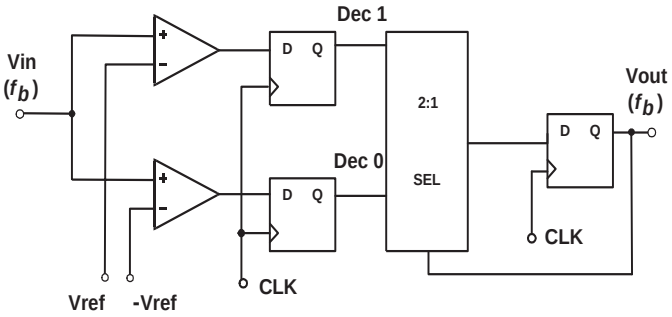


Fig. 2. Structure of type I

The simple parallel decision feedback loop of [5] and [6] shown in Fig. 2 (called type I later), adopts parallel data decision with different thresholds, therefore the delay of generating the analog threshold levels within the loop is avoided. But the components operate at the full data rate. The maximal delay limitation for the D Flip-Flop (FF) and the selector is only one bit period.

Feedback loop of [1] and 2] in Fig. 3 relaxes the timing constraints for components in feedback path by reducing the data rate of each channel by a factor of two, and both channels are coupled crosswise. Thus, the maximum input data rate is higher than type I.

Although this feedback loop (called type II later) in Fig. 3 can work without oscillation, the input data and the control signals of the two selectors are staggered in time. This causes unwanted pulse jumps at the output of the selectors which influence the data to be decided. To overcome this phenomenon, type III is proposed to synchronize the control signal and input data of both selectors (shown in Fig. 4). But the drawback of this structure is that the delay limitation in the feedback path is shortened to be half period of the CLK/2. To relax this delay limitation, type IV is proposed to enable the circuit operating at higher frequency. The detail will be discussed in part III.

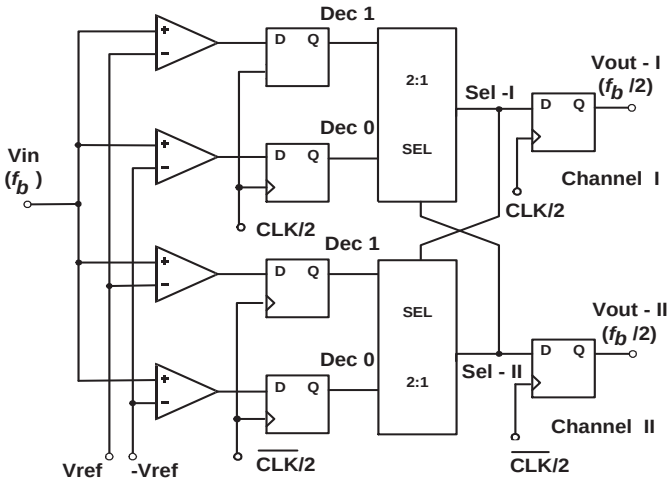


Fig. 3. Structure of type II

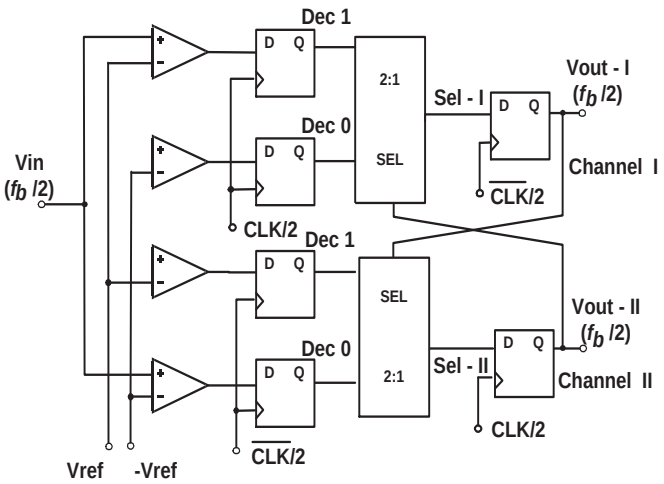


Fig. 4. Structure of type III

## III. Two new structures

In type II, we find that the control signals fed back from the selectors and the signals Dec1 and Dec0 being selected from both channels are staggered in each period. This causes an unwanted pulse jump transition at the output of selector.

The correct output data of the selector of, e.g., Channel I, should be sampled by the respective D-FF triggered by $CLK/2$ before the selector input change triggered by $\overline{CLK/2}$. The maximum input data rate depends on the bandwidth of the comparator, and the delay of the D-FF and the selector in the feedback loop. The minimal iput data rate is $1/\left(2\cdot\tau_{selector}+\tau_{D-FF}\right)$. Because if the sum delay of one D-FF and two selectors is smaller than $\frac{1}{2}T_{CLK/2}$, then the last D-FF will sample in the second half period of the selector, the decision would be wrong. This occurs only for low input data rate.

The above-mentioned drawback can be easily overcome by including the flip-flop in the feedback loop, however, at the price of speed. An alternative, termed type III, is illustrated in Fig. 4.

Instead of feeding the control signal from the node after the selector, the feedback signal is coupled from the output of the following D-FF. The control signal and the input data of the selector are synchronized by these two D-FFs which are triggered by the inverted clock compared to type II in Fig. 3. Therefore, the control signals of two channels have no chance to influence each other simultaneously. This scheme avoids unwanted pulse spikes after the selector. However, the delay limit for the D-FF and selector is within half period of CLK/2. Consequently, the maximum input data rate is comparable only to type I clocked at full clock rate.

With the intention to relax the speed limitation for the components in the feedback path of type III, type IV is proposed as shown in Fig. 5. The configuration of channel I in the upper part is same as that of type II, but in channel II, the data is sampled twice and then fed to the selector, the control signal and the input data of the selector are synchronized. In

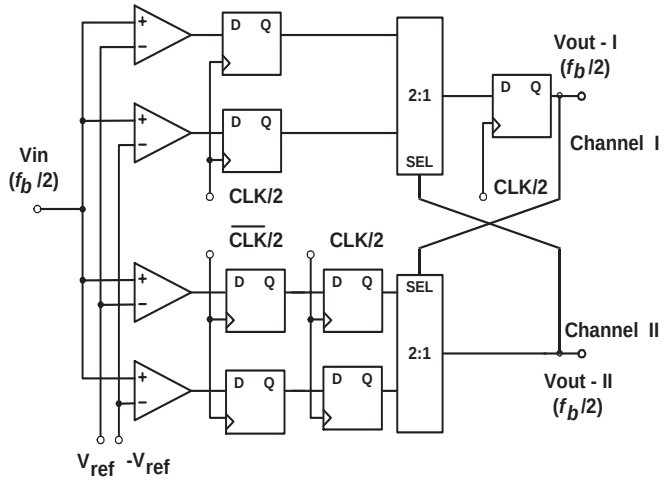


Fig. 5. Structure of type IV

channel I, the input data of the selector arrives earlier than the control signal of it. Although there are also spikes occurred at the output of the selector, the sampling instant of the following D-FF is away from the spike by $t_d$, which is the sum delay of D-FF and the selector. Here we see, type III combines the advantages of type II and type III. The improved performance will be shown in part IV.

## IV. Simulation results

The four types of decision feedback loops are designed and simulated by using the advanced SiGe:C Heterobipolar technology described in [8]. It is an epi-free and single-poly technology with 0.25 $\mu m$ minimum lithographic feature size and four metal layers. This technology incorporates low concentration of carbon into the SiGe region [9] of a heterojunction bipolar transistor (HBT) which significantly suppress boron outdiffusion caused by subsequent processing steps, and improves the HBT performance. The measured transit frequency $f_T$ and oscillation frequency $f_{max}$ are up to

200 GHz at breakdown voltage $BV_{CEO}$ $2.0\,V$, and extremely low ring oscillator delay 4.2 ps. The transistors are scalable with minimum emitter size 0.21×0.84 $\mu m^2$.

The circuits are simulated with pseudo random bit sequence (PRBS) input with ISI, and a comparison of the performances is summarized in Table I.

| Type | Input data rate (Gb/s) | Power (W) | Sum No. of Components |
|---|---|---|---|
| I | 0~60 | 1.17 | 6 |
| II | 15~90 | 2.25 | 12 |
| III | 0~60 | 2.25 | 12 |
| IV | 0~85 | 2.40 | 13 |

TABLE I

PERFORMANCES OF FOUR DECISION FEEDBACK LOOPS

For low input data rate, type I is very attractive for its low power, less components and small chip area. Type IV shows higher maximum input data rate than type I without speed limitation for low input data rate, and a little higher power consumption compared with type II.

## V. CONCLUSIONS

Four structures of decision feedback loop are analysed and compared in this paper. According to advantages and disadvantages of them, type I, II and IV are good choices for low and high input data rate respectively.

## VI. ACKNOWLEDGEMENT

The authors are very thankful for using the advanced 0.25 $\mu m$ SiGe:C Heterobipolar technology of IHP GmbH.

## REFERENCES

[1] L. Moeller, Z. Gu, A. Thiede, S. Chandrassekhar, and L. Stulz. : "20 Gbit/s electrical data recovery using decision feedback equalizer supported receiver," *Electron. Lett.*, Vol. 39. No.1, 9th Jan, 2003,

[2] Z. Gu, A Thiede, L. Moeller. : "20 Gbit/s decision feedback loop for optical communications," *European Gallium Arsenide Application Symposium*, Oct, 2003

[3] J. H. Winters, and R. D. Giltlin. : "Electrical signal processing techniques in long-haul fiber-optic systems communications," *IEEE Trans. Commun*. Vol. 38, No. 9, pp. 1439-1453, 1990

[4] L. Moeller, A. Thiede, S. Chandrassekhar, W. Benz, M. Lang, T. Jakobus, and M. Schelechtweg. : "ISI mitigation using decision feedback loop demonstrated with PMD distorted 10 Gbit/s signals," *Electron. Lett.*, Vol. 35, No. 24, pp. 2092-2093, 1999

[5] J. H. Winters, and S. Kasturia. : "Adaptive Nonlinear Cancellation for High-Speed Fiber-Optic Systems," *IEEE Journal of Lightwave Technology*, Vol, 10, No. 7, July,1992

[6] J. H. Winters, Richard. D. Gitlin, and S. Kasturia. : "Reducing the effects of transimission impairments in digital fiber optic systems," *IEEE Communication Magazine.* June, 1993

[7] S. Kasturia, and J. H. Winters. : "Techniques for high-speed implementation of nonlinear cancellation," *IEEE Journal of Selected Areas in Commnications.* Vol. 9. No. 5. June, 1991

[8] B. Heinemann, H. Ruecker, R. Barth, J. Bauer, D. Bolze, E. Bugiel, J. Drews, K. -E. Ehwald, T. Grabolla, and etc. "Novel collector design for high-speed SiGe:C HBTs," IEDM, 2002

[9] H. Joerg Osten, D. knoll, B. Heinemann, B. Tillack. : "Carbon doping of SiGe heterobipolar transistors," *Silicon Monolithic Integrated Circuits in RF systems*, Sep, 1998