A 16/17 Dual-Modulus Prescaler in SiGe HBT Technology

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***Abstract*— This paper presents the design of a 16/17 dual-modulus prescaler with maximum operating frequency of 30 GHz. The differential emitter-coupled logic (ECL) is employed to achieve high operating frequencies and high input sensitivity. The prescaler draws maximum 190 mA current with 3.3 V supply voltage. Compared with previous works [1], [2], [3], and [4], phase noise is emphasized and optimized.**

I. Introduction

In most communication systems, small channel spacing puts forward the requirement for frequency synthesizer to provide VCO frequencies with fine steps. Dual-Modulus prescaler, a key component of Phase-locked Loop (PLL), is a frequency divider with variable division ratios (N or N+1). This variable ratio enables the extension of the frequency range of using only programmable dividers.

In the meantime, as a key block of PLL, the prescaler affects the phase noise of PLL output significantly with the division ratio. This is emphasized in this work.

The aim of this work is to design a dual-modulus prescaler with division ratio of 16/17 and operating frequency as high as possible, with phase noise and power as low as possible based on the 0.5 μm SiGe HBT technology of Atmel. There is a trade-off among these factors in the design and the optimization of the circuit (Fig. 1).

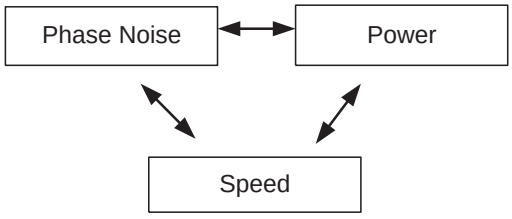

Fig. 1. Trade-off of prescaler design

II. Circuit Design

The block diagram of the dual-modulus prescaler in Fig. 2 consists of a synchronous divide-by-2/3 stage and an asynchronous stage with division ratio of 8. By combination with other logic gates, the division ratio of 16/17 is realized under the control of Modulus-Control signal.

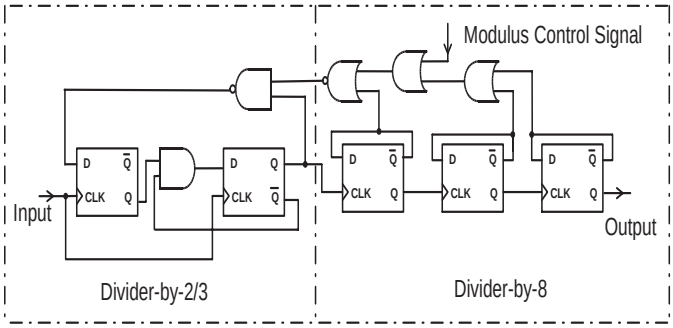

Fig. 2. Block diagram of prescaler

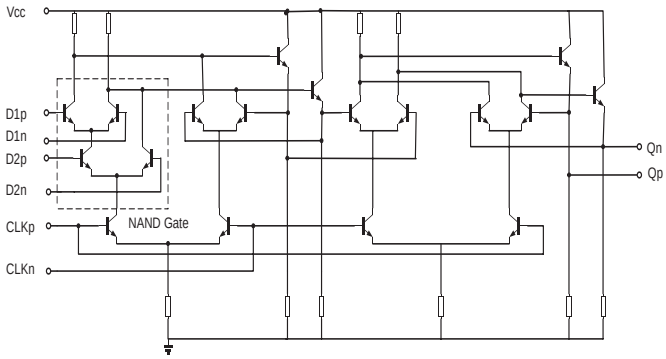

Fig. 3. Combination of NAND gates with master-slave D flip-flop

A divide-by-2/3 synchronous counter is used in this case instead of a divide-by-4/5 counter [3] to reduce the load capacitance of the input buffer of the clock signal. The maximum operating speed of the dual-modulus prescaler is mainly dependent upon the synchronous part. Therefore, the speed optimization is concentrated on this part with the price of large current. The combination of the logic gates with the divide-by-2 (Fig. 3) results in higher speed and low current consumption by sharing the current with the branch of divide-by-2.

Differential signals are fed into the whole circuits to reject noise and achieve good input sensitivity. ECL is adopted in the D flip-flop (FF), and emitter followers are added to speed

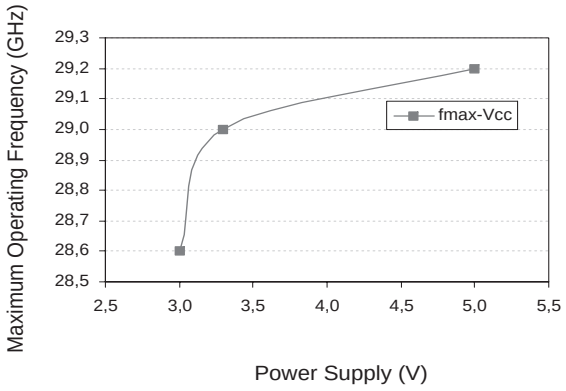

Fig. 4. Maximal operating frequency versus power supply voltage

up the circuit by keeping the transistors out of saturation and provide voltage level shift for the following stage. The low output impedance of the emitter followers also increases the number of the fan-out, and they are biased by current mirrors to provide constant current.

An improvement in one aspect of the performances may degrade performance in another. The maximum operational frequency of the prescaler is determined by the latches. ECL is preferred at high frequencies for two reasons. First, fast switching is feasible with ECL latches. Secondly, there is a proportional relation between the power consumption P and circuit parameters

$$P \propto C \cdot V_{pp} \cdot V_s \cdot f \tag{1}$$

C is the total capacitance, V_{pp} is the voltage swing, and V_s is the power supply, f is the operating frequency. Small voltage swing can greatly reduce the power consumption at higher frequencies. Therefore the voltage swing of the output is optimized to be large enough to be detectable for the next stage at the highest frequency.

With a larger supply voltage, there is larger noise margins for the output voltage swing. However, it is not necessary to increase the maximum operating frequency a little with the price of using 5 V. The simulation for divider-by-2 is shown in Fig. 4. Therefore, the optimal 3.3 V power supply is adopted, and the output voltage swing is optimized to achieve minimal power.

In PLL, the frequency divider is often followed by edge-triggered circuit such as Phase/Frequency Detector (PFD), which is a threshold sensitive circuit. The noise from the logic devices will be edge jitter noise. Division by N corresponds to (N-1) periods being swallowed when N periods are transmitted in the time domain. This down-sampling in time domain causes folding in frequency domain. This means the noise behavior of PLL is greatly influenced by the frequency divider when the threshold is being crossed. The phase noise due to accumulation can be expressed as:

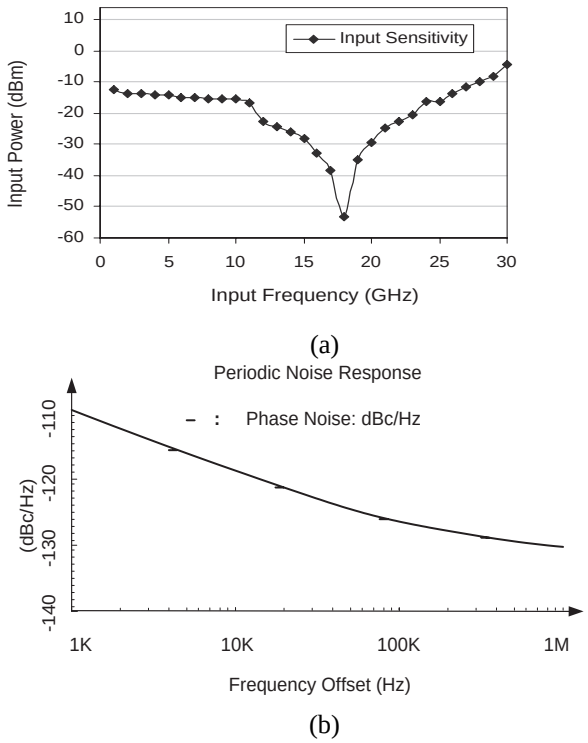

Fig. 5. Simulaton of (a) input sensitivity (b) phase noise

$$S_{\phi_{out}} = \frac{1}{T_K^2} \sum_{k=0}^{K} T_k^2 \cdot S_{\phi_k} \tag{2}$$

The signal from VCO feeding to the prescaler can be expressed as:

$$S(t) = V(t) \cdot \cos[\omega_0 t + \theta(t)] \tag{3}$$

Where $V(t)$ describes the amplitude variation as a function of time and *θ(t)* the phase variation. *θ(t)* is referred to as phase noise. For a high-quality oscillator, the amplitude is very stable, and $V(t)$ can be considered constant. Then a carrier signal of amplitude V and frequency f_0, which is frequency-modulated by a sine wave of frequency $f_{m,}$ can be expressed by:

$$S(t) = V \cdot \cos[\omega_0 t + \frac{\Delta f}{f_m} \sin(\omega_m t)] \tag{4}$$

in which Δf is the peak frequency deviation and $\theta_p = \omega_0 t + \frac{\Delta f}{f_m}$ is the peak phase deviation. From the equation (4), the instantaneous phase $\theta_i(t)$ of a carrier frequency modulated by a sine wave of frequency f_m is

$$\theta_i(t) = \omega_0 t + \frac{\Delta f}{f_m} \cdot \sin(\omega_m t) \tag{5}$$

Instantaneous angular frequency is defined as the time derivative of the phase:

$$\omega = \frac{d\theta_i}{dt} = \omega_0 + \frac{\Delta f}{f_m} \cdot \omega_m \cdot \cos(\omega_m t) \leq \omega_0 + \Delta\omega \tag{6}$$

If this signal is fed into the frequency divider with division ratio N, the output frequency ω_0 is expressed as

$$\omega_0 = \frac{\omega_0}{N} + \frac{\Delta\omega}{N} \cdot \cos(\omega_0 t) \tag{7}$$

The output phase is:

$$\theta_i(t) = \frac{\omega_0 t}{N} + \frac{\Delta f}{N \cdot f_m} \cdot \sin(\omega_m t) \tag{8}$$

The frequency divider reduces the frequency by N, the peak phase deviation is also reduced by N. The ratio of the noise power to carrier power is:

$$(\frac{V_n^2}{V})^2 = \frac{\theta_p^2}{4} \tag{9}$$

Based on this analysis, the influence on the phase noise of PLL is 20log(N) dBc/Hz from the prescaler.

While the phase noise of the synchronous part is not related to the number of the stages and only influenced by the noise of the clock and previous stages. Therefore, the optimization for high speed is concentrated on the synchronous part because this part deals with the highest frequency. In contrary to this, the asynchronous part shows clock jitter, the phase noise optimization is of great importance.

III. Simulation and Measurement Results

The dual-modulus prescaler is designed by using 0.5 μm SiGe HBT technology with transit frequency f_T of 80 GHz and oscillating frequency f_{max} of 90 GHz. The maximum operating frequency is up to 30 GHz from the simulation in Agilent ADS (Fig. 5(a)). It draws about 190 mA current with 3.3 V voltage supply. The input sensitivity is good to be -50 dBm at the self-oscillating frequency 18.8 GHz, and the phase noise of the prescaler is -123 dBc/Hz at the offset frequency 10 KHz in Cadence simulation in Fig. 5(b). The layout of the prescaler is shown in Fig. 6, the size is 0.6×0.5 mm^2.

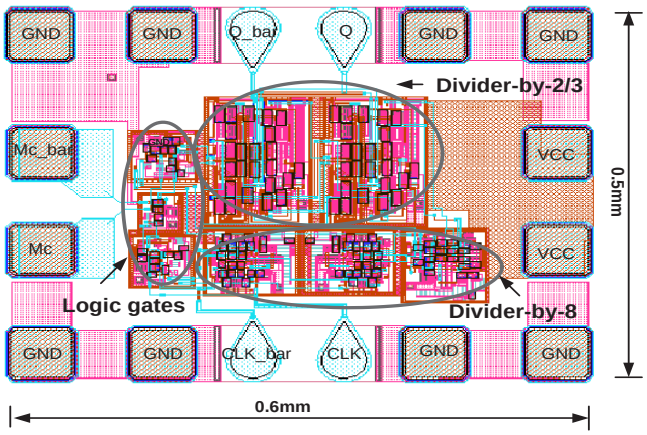

Fig. 6. Layout of prescaler

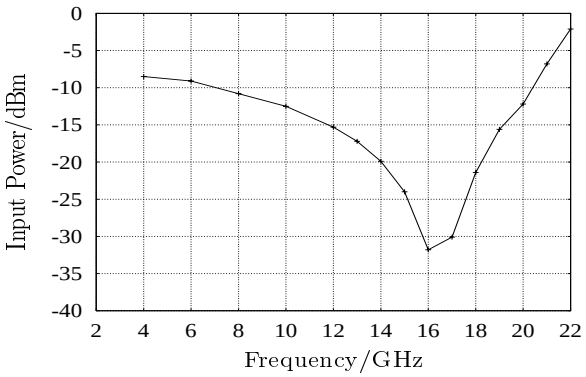

Fig. 7. Measured input sensitivity

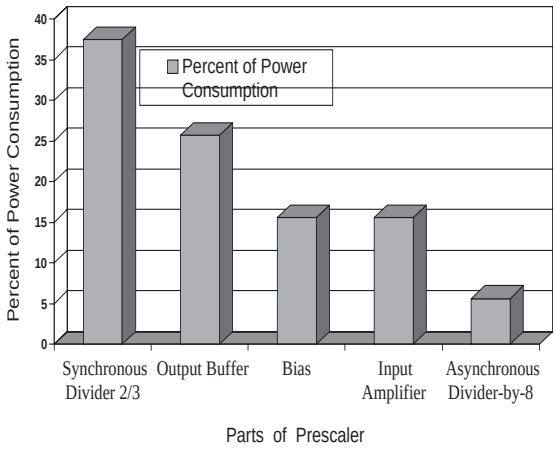

Fig. 8. Power distribution of each part of the prescaler

One of the divider-by-2 blocks in the asynchronous part is measured, the input sensitivity is shown in Fig. 7. The measured maximum operating frequency is up to 22.3 GHz, compared to the simulated maximum operating frequency 26.4 GHz, only drops by 4 GHz.

Based on different optimization focus on each part of the prescaler, a summary of the power distribution is shown in Fig. 8. It is clear that the synchronous parts consumes the largest part of power dealing with the highest frequency, while the asynchronous part consumes the least power in the whole circuits. Table I gives a summary of the prescaler data.

IV. Conclusions

A dual-modulus prescaler has been developed to meet the requirement of the system by providing the highest operating frequency and as low as possible power. In the meantime, the phase noise of this component is emphasized and optimized in this work.

Technology	0.5 μm SiGe HBT
Supply voltage	3.3 V
Divide ratios	16/17
Supply current	190 mA
Output voltage	> 0.4 V_{pp}
Maximum input frequency	30 GHz
Chip size	0.6*0.5 mm^2

TABLE I

TECHNICAL DATA OF PRESCALER

REFERENCES

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