30 Gb/s Parallel Optic-Fiber Receiver ICs Design*

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Abstract

A 30 Gb/s parallel optic-fiber receiver structure is presented. Parallel receiver amplifiers of 12 channels have been designed using TSMC 0.25 μm CMOS technology and for single-channel bit rate of 2.5 Gb/s. The total DC current of the parallel receiver amplifiers is about 0.54 A at a 3.3-V supply, corresponding to a power consumption of 1.78W. The voltage swing at each single-end output is 400 mVp-p.

1. Introduction

As telecommunications and data-communications rapidly developed, optic-fiber networks are widely implemented. The continuous increase in communication speed has motivated the design and implementation of optic-fiber networks in high speed and high capacity, and these performances can be satisfied by parallel optic-fiber transmission systems.

Our 30 Gb/s parallel optic-fiber receiver consists of 12 channels with 2.5 Gb/s per channel. Each channel includes a transimpedance amplifier followed by a limiting amplifier. At such a high bit rate, the amplifier can be manufactured easily by using a GaAs or a silicon bipolar technology, but with a higher cost. Advanced CMOS technologies are attractive from standpoints of integration, power, and cost. With the feature size scaling down to 0.25 μm and below, the CMOS technology is becoming the most interesting process for optic-electronic integrated circuits. So our 30 Gb/s parallel optic-fiber receiver ICs are designed in 0.25μm CMOS technology.

2. System Structure

As shown in Fig.1, our 30 Gb/s parallel optic-fiber receiver includes 12 parallel channels with each channel working at 2.5 Gb/s. The system consists of a micro-optics module, 12 parallel photodetectors and 12 parallel receiver amplifiers. The micro-optics module couples the optical signals from 12 parallel optic-fibers onto 12 parallel photodetectors. The parallel photodetectors convert the optical signals into electrical signals. The parallel receiver amplifiers amplify the small signals from photodectors with a high enough gain but a low noise factor.

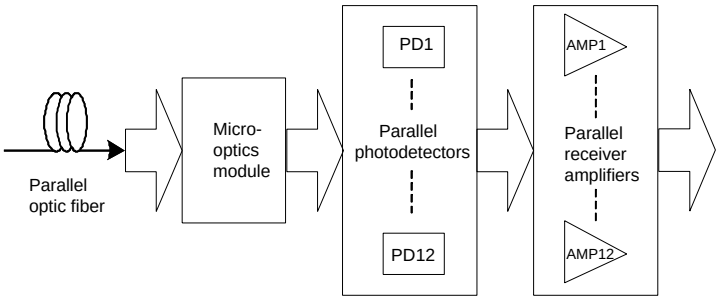

Fig.1 Parallel optic-fiber receiver structure

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3. Receiver Amplifiers

There are 12 receiver amplifiers in parallel. Each amplifier combines a transimpedance amplifier as preamplifier and a limiting amplifier as main amplifier. These amplifiers were designed in TSMC 0.25 µm CMOS technology.

3.1 Transimpedance Amplifier (TIA)

The basic circuit of the transimpedance amplifier designed is shown in Fig.2. It plays a critical role in optical receivers. Trade-offs between noise and gain-bandwidth characteristics present many challenges in the design. Thus, it is optimized for both the minimum noise and the maximum achievable gain in defined bandwidth, what is important for high efficiency of the receiver [1, 2].

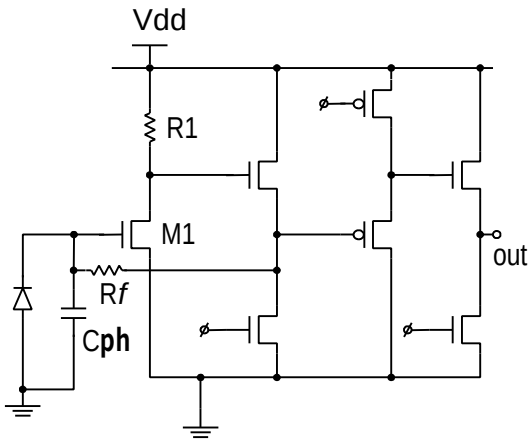


Fig. 2 Circuit diagram of transimpedance amplifier

The TIA bandwidth is typically chosen to be equal to 0.8 time of the bit rate of a single channel (2.5 Gb/s) – a reasonable compromise between the total integrated noise and the intersymbol interference (ISI) resulting from limited bandwidth. The TIA bandwidth is designed for 2 GHz for C_{ph}=0.5 pF.

Fig. 3 shows the equivalent input referred noise current spectral density as a function of the size of MOSFET M_1, at 2 GHz for a fixed feedback resistor of 500 ohm. The optimum gate-width of M1 was found to be 62 µm. The simulated equivalent input current noise spectral density as a function of the frequency is shown in Fig. 4. The simulation results of TIA with 62 µm gate-width of M1 give a bandwidth of 2.1 GHz and a transimpedance gain of 51 dBΩ with 1 µA input current at 2.5 Gb/s.

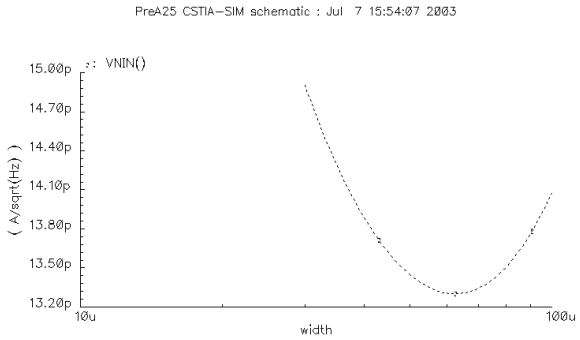


Fig. 3 Equivalent input referred noise current spectral density as a function of the gate width of M_1 at 2 GHz

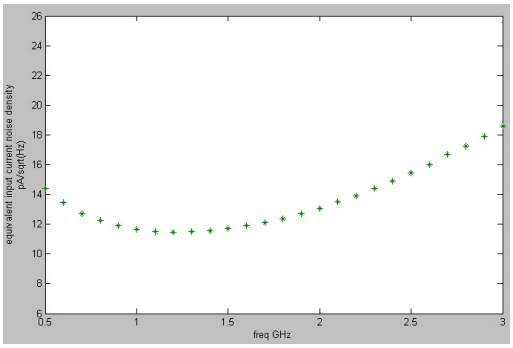


Fig. 4 Equivalent input current noise spectral density of TIA

3.2 Limiting Amplifier

The limiting amplifier shown in Fig.5 has a DC coupled, fully differential circuit. It consists of an input buffer, three similar amplifier cells, an output buffer for driving 50Ω load, and a pair of total feedback networks for offset canceling [3]. The whole circuit is fully balanced. The non-linearity of differential current amplifiers is used for the limiting function. The three amplifier cells have the same circuit as shown in Fig.6.

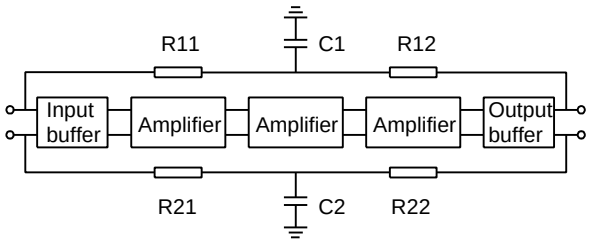


Fig. 5 Block diagram of limiting amplifier

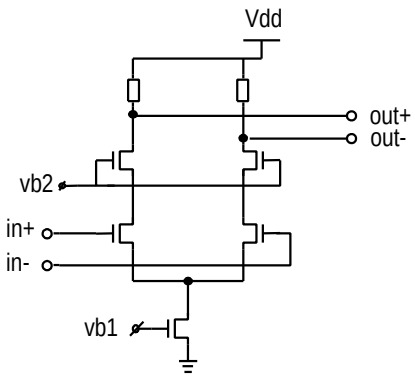
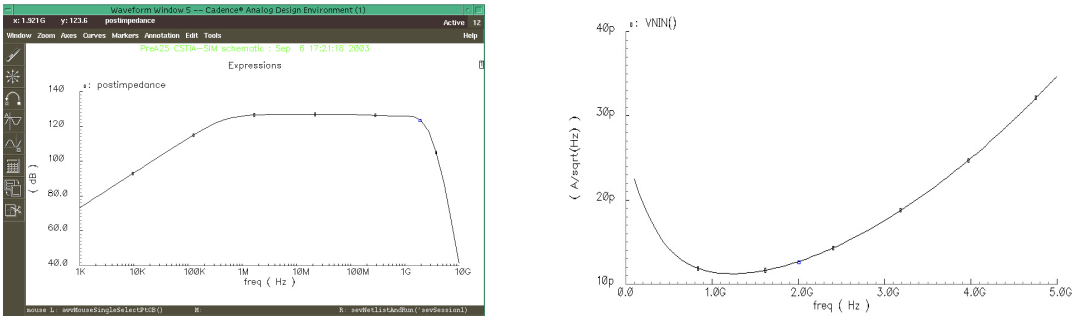


Fig. 6 Circuit diagram of an amplifier cell

3.3 Simulation

Between the transimpedance amplifier and the limiting amplifier, an interface circuit is inserted to make the transformation of single-ended to differential structure. The receiver amplifier has been simulated with 1 μA input current using Cadence as shown in Fig.7 (a) for frequency response and Fig.7 (b) for input referred noise current density. Simulation results have shown that a flat response over 2 GHz and total gain of 128 dBΩ can be obtained. The input referred noise current

density of the receiver amplifier was 16.9×10^{-23} A^2/Hz at 2 GHz.



(a) Frequency response (b) Input referred noise current density

Fig. 6 Simulation results of the receiver amplifier

4. Layout Design

The parallel receiver amplifiers have been realized in a 0.25 μm CMOS technology of TSMC. The layout of 30 Gb/s parallel receiver amplifiers is shown in Fig.7. Isolation between two neighboring channels was used for avoiding the interference of them.

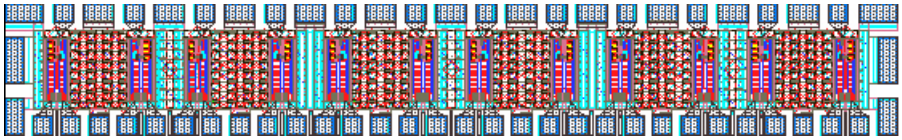


Fig. 7 Layout of 30 Gb/s parallel receiver amplifiers with 12 channels

5. Conclusion

A structure of 30 Gb/s parallel optic-fiber receiver is presented. It is designed in a 0.25 μm CMOS technology. The circuit is taped-out, and the test results will be given later.

References

1. Tongtod Vanisri, Chris Toumazou, “Integrated High Frequency Low-Noise Current-Mode Optical Transimpedance Preamplifiers: Theory and Practice”, IEEE Journal of Solid-State Circuits, Vol.30, No.6, June 1995
2. Z.-G. Wang, X.-H. Chen, and al. “2.5-Gb/s 0.35-μm CMOS ICs For Optic-Fiber Transceiver” ICECS’2001, Sept. 2-4, 2001, Malta
3. Rui Tao, Zhi-Gong Wang, Ting-Ting Xie, Hai-Tao Chen, Yi Dong, Shi-Zhong Xie，“A CMOS Limiting Amplifier for SDH STM-16 Optical Receiver, ”Electronics Letters，Vol. 37, pp. 236-237, 2001