Device Simulation of Double Photo-diodes

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Abstract: Photo-generated carriers' transmission delay of a CMOS-Process-Compatible double photo-diode（DPD）is analyzed by using device simulation in this paper. The carriers' transmission delay of a DPD in CMOS N-well process is made up of three parts: the delay in the P^+ region, depletion region and N-well. The diffusion delay is relative to the depth, the doping concentration of the N-well and the bias. The frequency characteristic is obtained by simulating the DPD with different bias voltage, depth and doping concentration of the N-well. Adopt smaller size CMOS process is benefit to improving the speed due to the shallow well.

Keywords: double photo-diode（DPD）, optoelectronics integrated circuit (OEIC), photo-detector, Device simulation, OEIC receiver

1. Introduction

Silicon based photo-detector can be widely used in short wavelength (i.e.0.78~0.85um) optical system, such as in Gigabit Ethernet and fiber channels. To achieve high speed and high volumes in optical communications, optoelectronics integrated circuit (OEIC) is the ultimate way, because the OEIC eliminates the parasitic effects induced by hybrid integration. This technology also has advantages of reducing chip area, achieving higher yield and higher reliability.

A CMOS process-compatible DPD is recently reported in [1,2]. The responsivity of the DPD is about 0.01~0.04A/w at 850nm. Operating at 1.25Gbit/s, the OEIC receiver including the DPD requires an incident optical power of -6.3dBm to obtain a measured bit error rate of 1×10^{-9}.

The DPD uses the P^+ source/drain implant and N-well in CMOS process to construct an operation diode, and uses the N-well and the P substrate to constitute a screen diode. The screen diode minimizes the effect of slow diffusion of photo-generated carriers from the substrate, which results in the DPD's high speed detectability. In general, the junction capacitance is considered as the most significant factor that limits speed of the receiver, and the delay of photo-generated carriers can be ignored. However, the DPD does not always work like the PIN diode, and sometimes the delay of photo-generated carriers may be longer than the delay caused

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by junction capacitor. With the help of device simulation, this paper analysis the mechanism of photo-generated carriers' transmission delays and gives frequency characteristic of the DPD under different conditions. Atlas, a commerce program, is used in implementing the device simulation.

2. Device simulation and analysis of operating principle

(1) Device structure and mechanism of transmission delay

To fabricate the DPD, an N-well surrounded by a grounded P^+ guard ring is employed in the P-substrate. And an interdigitated network of P^+ region, which is formed at the same time as the source/drain of PMOS device, is implanted in the N-well. A cutaway diagram of the DPD structure is shown in Fig.1, where, the junctions' position and the depletion regions under external bias are also included by two-dimensional simulation. The junction formed by N-well and P^+ is called the operation diode(D_o), and the other one formed by N-well and P-substrate is the screen diode(D_s). Both D_o and D_s are reversely biased when the DPD works normally. It means that N^+ electrode should be applied to a positive bias, the P^+ guard ring be grounded and the P^+ electrode is the output. The photo-generated carriers which are far from D_o are screened by the depletion region of D_s and can not diffuse from substrate to D_o. Only the carriers which are generated in N-well can diffuse to D_o and their diffusion distance is very

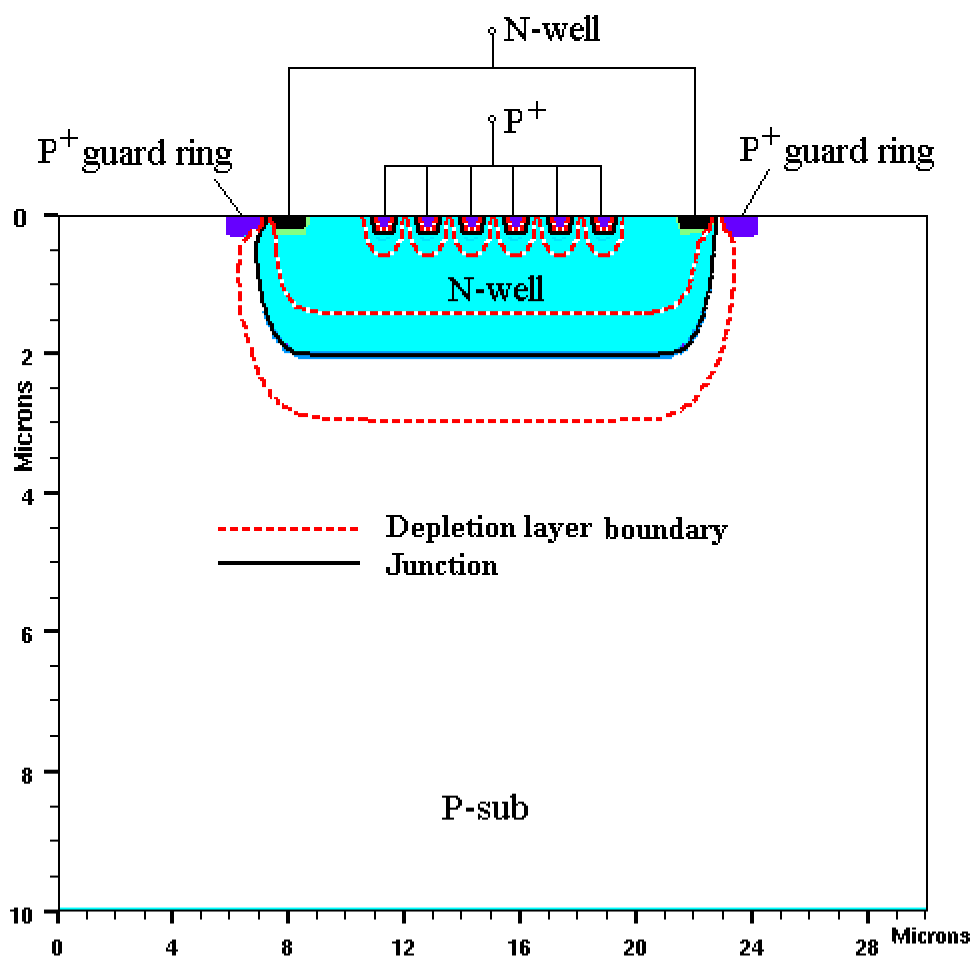

Fig. 1 Structure, pn junction position, depletion layer of the DPD in two dimension device simulation and the sketch map of electrodes

short. Therefore D_o's speed is improved. In order to minimize the diffusion part of photo-generated carriers the D_o's depletion region need to be as wide as possible, and a light doping N-well region is required to obtain an ideal intrinsic layer. But it is difficult to realize in actual CMOS process, for the impurity density of the N-well is much higher (about 10^7). Operating at a normal bias, D_o is still a P^+N diode rather than a PIN diode because it doesn't deplete fully, and its speed is limited due to the diffusion portion of carriers in N-well.

Fig.2 shows the vector-graph of the total current density when the DPD is illuminated.

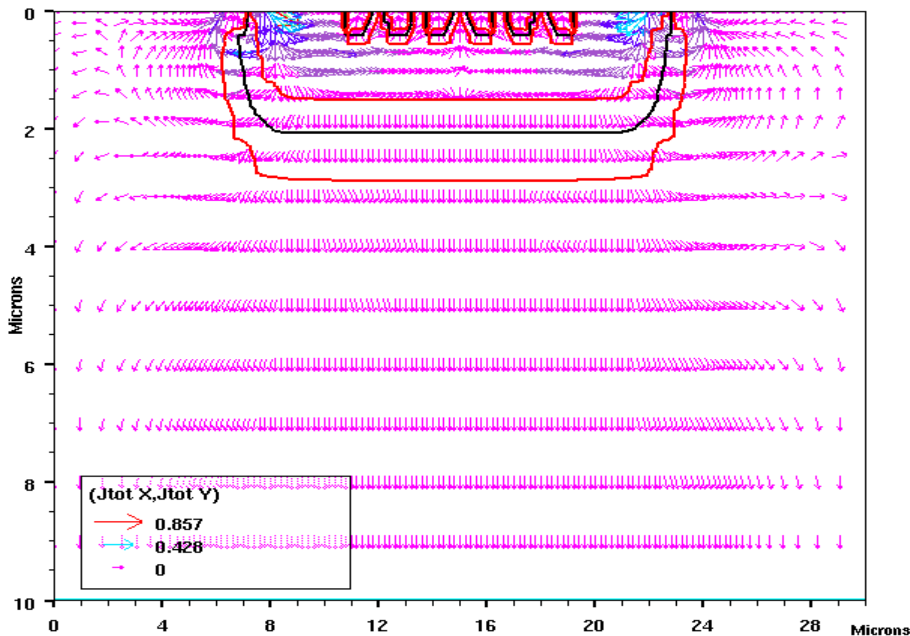

Fig. 2 vectorgraph of the total current

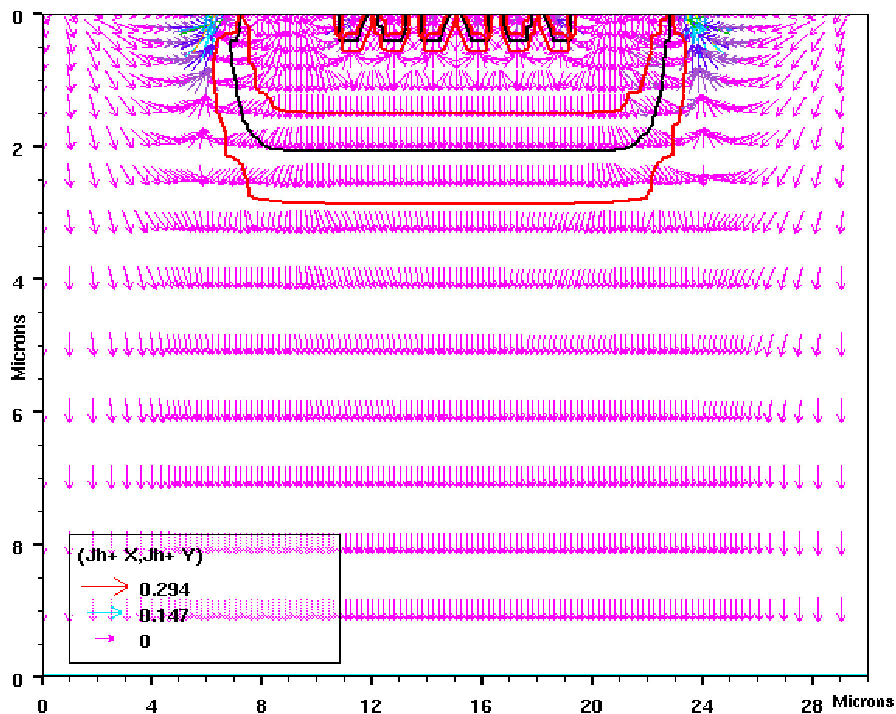

Fig.3 vectorgraph of the hole current density of the DPD

The photo-generated carriers that are far from the depletion region of D_o flow to D_s, the P^+ guard ring and the substrate. Those carriers can't reach at D_o and don't contribute to the photo-current, so diffusion time is reduced and the speed of D_o is improved. The photo-generated carriers within a minority diffusion length near the PN junction of D_o in N well diffuse to the depletion region of D_o, which form the diffusion current. This part of carriers is the main factor that limits the speed of D_o because they are diffusion current.

Fig.3 shows the vector-graph of the hole current density when the DPD is illuminated. From the chart we can see that the part of photo-generated carriers (holes) which diffuse to D_o contribute to operation current, and those diffuse to D_s are no use to operation current.

From the above analysis, we know that photo-current are made up of three parts of carriers: carriers generated in the P^+ region, depletion region and N-well, respectively (see Fig.2). Contributions of these three parts to the total current are different:

1) Electrons (minority) of the photo-generated carriers within a diffusion length in P^+ region can diffuse to the operating depletion region, which form the diffusion current of P^+ region. However the P^+ region is very shallow when it is fabricated in CMOS process, therefore the minority diffusion distance is very short, and the delay time can be neglected.

2) Under the reverse bias, the electrons of photo-generated electron-hole pairs drift to N-well, and the holes drift to P^+ region, which form the drifting current. Moreover, the carriers transmitting distance is short because of the shallow depletion layer of the D_o. So this delay time is very small, and it can be ignored too.

3) Holes (minority) of photo-generated carriers within a diffusion length in N-well, which form diffusion current, diffuse to two depletion regions simultaneously (see Fig.3). The carriers diffusing to the operating depletion region contribute to the total current, but because of the relatively long diffusion path, they are the most significant factor determining the delay time of a DPD.

(2) Frequency characteristic simulation

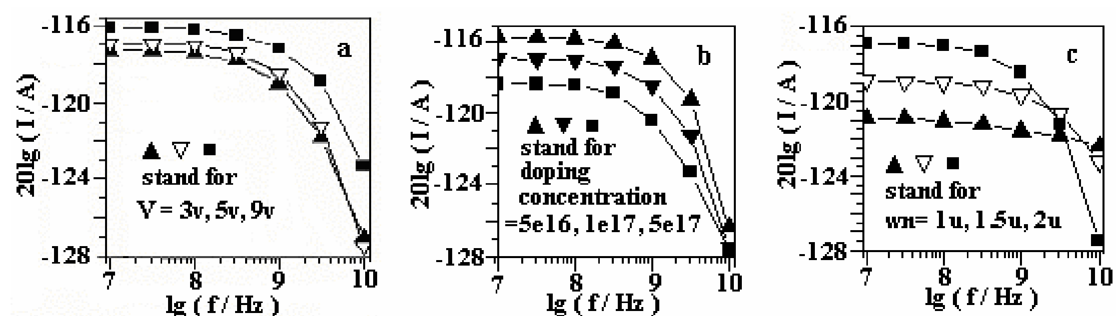

Fig. 4 frequency response: (a) with different bias voltage, (b) with different doping concentration, (c) with different depth of the N-well

Fig.4(a) shows the frequency response of a $20\times20\mu m^2$ DPD with different bias voltage when the doping concentration of the N-well is 1e17 and the depth of the N-well is 2u. The intensity of incident light is $25W/cm^2$. It can be seen from the chart

that as the bias voltage increases, both of the -3dB bandwidth of the DPD and the total current increase. Because the depletion region becomes wider with larger bias voltage, the drifting current increases and the diffusion current reduces that increase the bandwidth. Moreover, we can see that the increment of the drifting current is larger than that of diffusion current, so the total current increases.

It is shown the frequency response of the DPD with different doping concentration of the N-well in Fig.4(b) when the bias voltage is 5v and other parameters are the same as fig.4(a). We can see that as the concentration reduces, both of the -3dB bandwidth of the DPD and the total current increase. That is because the width of the depletion region increases as the concentration reduces, and the result of the wider depletion region is just as the discussion of Fig.4(a).

Fig.4(c) shows the frequency response of the DPD with different depth of the N-well (w_n) when the bias voltage is 5v and other parameters are the same as fig.4(a). It can be seen that when the w_n increases, the -3dB bandwidth reduces, whereas the total current increases. Because the deeper N-well results in the increase of the diffusion distance, the bandwidth reduces. Moreover, as the w_n increases, the light absorption depth increases and there are more photo-generated carriers, so the total current is larger.

3. Conclusions

The characteristic of the DPD relates notablely to the bias voltage and the CMOS process. But different CMOS process has different depth and doping concentration of the N-well. The bias voltage, the depth and doping concentration of the N-well, as described above, are the factors of limiting DPD's speed, which must be taken into account enough in designing.

References

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