

SHORT COMMUNICATION

Properties of Coplanar Type MIS-SIM Structure Chip Capacitor

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In MIS-structure, the capacitance depends on applied voltage and its polarity,¹ temperature,² oxide thickness and doping level of semiconductor.³

Coplanar type MIS-SIM structure has been designed and fabricated on low resistivity silicon. The two electrodes are deposited on the thermal oxide grown on silicon. This structure could be analysed by connecting an MIS structure in series with a SIM structure, thus minimising the voltage and temperature variations on capacitance of the MIS-SIM structure as compared to MIS structure. The coplanar type can be used as a discrete capacitor as well as for hybrid circuits where low VCC & TCC are required.

FABRICATION

Polished *n*-type silicon wafer of resistivity 0.01 ohm-cm was taken and SiO₂ was grown thermally at 1150°C. Electrodes pattern were deposited by evaporating 99.999% Aluminium at 10⁻⁶ torr vacuum through molybdenum mask. The substrate temperature was kept at 125°C during deposition of elec-

trodes. The wafer was scribed and diced. The chips were die mounted and wire bonded on TO-5 packages. The capacitor structure is as shown in Figure 1.

MEASUREMENTS AND RESULTS

The capacitance of the encapsulated chip capacitor was measured at 1 KHz. The bias voltage during the capacitance measurement was varied from 0 to ±100V and no change in the capacitance value was observed within a measurement accuracy of 0.025%. The capacitor was mounted on a temperature jig so that its temperature could be increased from room temperature to 150 degree centigrade. The change in capacitance was less than 5 ppm/degree centigrade. Results are summarised in Table I for the varying oxide thickness of the proposed structure.

In an MIS structure, the capacitance varies with temperature² as shown in Figure 2(a). The variation is due to the change of the Fermi level in the semiconductor as shown in Figure 2(b). At T_1 the Fermi level is assumed to be above the surface states, which are filled with electrons and are neutral. When the temperature is decreased to T_2 , the Fermi level moves closer to the valence band and some of the surface states lose electrons and become positively charged. However, it is assumed that the permittivity of SiO₂ dielectric does not vary with temperature.⁴ In the coplanar MIS-SIM structure, the change of Fermi level for the MIS structure due to temperature would be in the opposite direction to the SIM structure, and thus the temperature effect would be minimised.

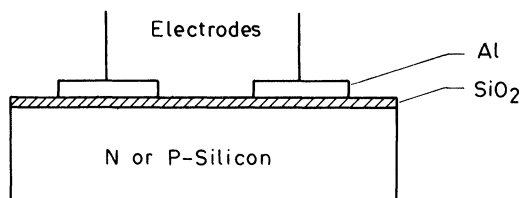


FIGURE 1 Structure of coplanar type MIS-SIM capacitor.

TABLE I

Sr. No.	Oxide thickness	Capacitance	No. of capacitors.	TCC	VCR
1.	0.1150 μm	210–220 pf	10	5 ppm/C	0
2.	0.3 500 μm	68–73 pf	10	3 ppm/C	0
3.	0.5 000 μm	45–48 pf	10	3 ppm/C	0

Chip area : 100 mils \times 100 mils

Electrode Area : 85 mils \times 36 mils

Separation between Electrodes : 14 mils

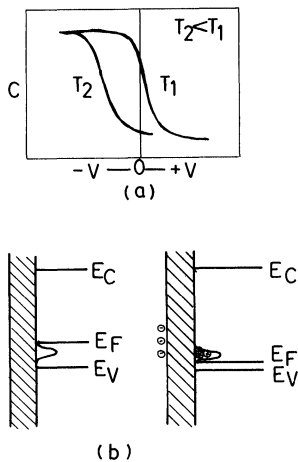


FIGURE 2 (a) Capacitance variation of an MIS structure with temperature. (b) Simplified band structure showing change of Fermi level due to temperature (Ref. 2).

The coplanar type MIS-SIM structure chip capacitor is of high quality and is almost independent of changes in voltage and temperature.

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