A Novel Current Memory Circuit for AMOLEDs

Yen-Chung Lin and Han-Ping David Shieh

***Abstract*—A novel switched-current (SI) memory circuit with improved accuracy and operating frequency for active-matrix organic light-emitting displays (AMOLEDs) was developed. The proposed SI memory, constructed from current memory structure, can not only reduce the influence of charge-injection without using larger storage capacitor, but also realize the significant amount of speed up by means of small storage capacitor. Furthermore, the capability of copying the current signal is achieved without relying on the matching of device characteristics. The proposed SI memory circuit was implemented by low temperature poly-silicon technology and is suitable for current driving scheme-based high-resolution AMOLED applications.**

***Index Terms*—Active matrix, active matrix organic light-emitting displays (AMOLEDs), current memory, low temperature poly-silicon thin-film transistors (LTPS-TFT), organic light-emitting displays (OLEDs), switched current.**

I. Introduction

Organic light-emitting displays (OLEDs) have attracted enormous attention because of their potential flat-panel display applications. Active matrix addressing is eminent for high information content displays. A great deal of research and development in this field has been published based on the low-temperature poly-silicon thin-film transistor (LTPS-TFT) technologies [1]–[4]. Ensuring the brightness uniformity of each pixel is essential for acquirements of high quality images of LTPS-TFT active-matrix organic light-emitting displays (AMOLEDs). The variations of device characteristics caused by device aging or manufacturing process are still an issue in LTPS-TFT technology. More specifically, the variations of threshold voltage can affect the drain current and result in the nonuniform phenomena. Due to the variation of device characteristics, the current driving technology with self-compensation function of AMOLEDs is the leading scheme for achieving the uniform image quality [5].

The switched-current (SI) memory has been widely used in analog sampled-data signal processing applications [6], [7], since they exhibit superior tolerance to device parameter variations. One of the fundamental factors limiting an accuracy of the SI memory is the charge injection occurring when the transistor turns off [8]. The amount of charge a TFT carries in its channel when the gate voltage applied can be expressed as

$$Q_{\mathrm{ch}} \approx \mathrm{WLC_{OX}}(V_{\mathrm{GS}} - V_{\mathrm{TH}}).$$

As the TFT turns off, this charge is released from the channel to the source and drain (S/D) terminals and affects the voltage at both these terminals.The voltage offset appears as a nonlinear term at S/D terminals because Q_{ch} is interrelated to the S/D voltage. The accuracy of SI memory depends upon how to protect the critical gate voltage when the voltage builds up due to the variation of gate voltage causing the reproduced current to be different from the input current. The low sensitivity to the charge injection mechanism of SI memory can be realized by several methods such as:

Manuscript received December 2, 2003; revised February 17, 2004. The review of this brief was arranged by Editor J. Hynecek.

The authors are with the Institute of Electro-optical Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.

Digital Object Identifier 10.1109/TED.2004.827371

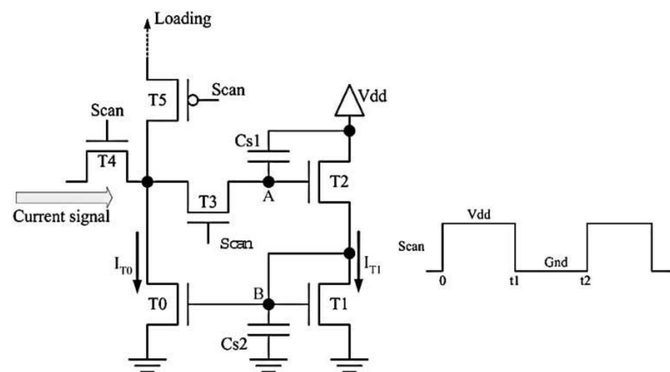

Fig. 1. Schematic diagram of proposed SI memory. The circuit samples the current signal in the interval $0 < t < t_1$. The circuit reproduces the sampled current in the interval $t_1 < t < t_2$.

1) the usage of complementary switch for the partial cancellation of the charge injection; and
2) the usage of large capacitance for the reduction of the voltage offset at critical node.

The first method eliminates the charge injection in terms of the carriers that cancels each other due to the opposite polarities (such as those from n-TFT and p-TFT in the complementary switch). However, the requirement of additional clock signals increases the amount of connecting wire and control logic as well as the complexity of the control system. Besides, the parasitic capacitance of connecting wire may induce the clock signals misalignment and lose the capability of charge injection cancellation. The other way is increasing the storage capacitance to contain the effect of the charge injection. Nevertheless, the larger storage capacitance requires more charging time to establish the gate voltage during the sampling period, consequently decreasing the operating frequency.

In this brief, a current mirror-based SI memory restraining charge injection with one control signal is proposed and designed. The experiment results of SI memory implementation using LTPS-TFT process are also presented.

II. Circuit Description

Proposed SI memory designed with current mirror is capable of protecting the critical gate voltage against disturbed by charge injection, as shown in Fig. 1. The TFT T0, T1, and T2 build the current mirror, and T3, T4, and T5 act as the switches. Two capacitors Cs1 and Cs2 are used as storage capacitors. The proposed SI memory operates in two modes: sampling and reproducing.

1) Scan $= V_{\mathrm{dd}}$. The SI memory is connected to external current source by T4. The drain-to-gate voltage of T2 is adjusted roughly to generate the current I_{t1}. Then I_{t1} sets the the gate voltage of T0 to an appropriate value for generating the current I_{t0} as the same as the input current.
2) Scan = ground. The SI memory is connected to the loading by T5 and has a capability of sinking the approximately equivalent current from the loading. T1, T2, and T3 make contribution to functionally protect the critical gate voltage of the SI memory. As the scan signal goes to ground, it turns off transistor T3, thereby, driving the circuit into reproducing mode. The charge carriers stored in the channel of T3 is released and redistributes to the gate of T2 (node A). Therefore, the charge carriers injecting into the storage capacitor results in the gate voltage variation of

0018-9383/04$20.00 © 2004 IEEE

TABLE I
PARAMETERS FOR SI MEMORY DESIGN

Device	
W/L for T0, T2, T3, T4, T5 (μm)	7/5
W/L for T1 (μm)	7/5, 15/5, 30/5, 50/5
Loading circuit	Pixel liked active loading
Cs (fF)	100, 200, 400, 800
μ_n (cm^2/V-sec)	77.4
μ_p (cm^2/V-sec)	85
Supply Signal	
Vdd, logic-High (V)	10
Ground, logic-Low (V)	0
Input current (μA)	0.1 ~ 12

$T2$ (ΔV_A). A parameter $g_m \cdot V_{\rm GS}$, with the transconductance g_m defined in saturation region as

$$g_m = \frac{\partial I_D}{\partial V_{\rm GS}} = \left(2I_d \cdot C_{\rm OX} \cdot \mu \cdot \frac{W}{L}\right)^{\frac{1}{2}} \tag{1}$$

is one of the important parameters of the TFT in the voltage-controlled curent source circuit. The current I_{t1} deviates from the input current due to the gate voltage variation of T2 (ΔV_A) of $g_{m2} \cdot \Delta V_A$ as shown in (2), where g_{m2} is transconductance of T2

$$\Delta I_{T1} = g_{m2} \cdot \Delta V_A. \tag{2}$$

The current I_{t1} through T1 is changed by charge injection mechanism so that the voltage at node B is also altered as follows:

$$\Delta V_B = \frac{\Delta I_{T1}}{g_{m1}}. \tag{3}$$

To combine (2) and (3), the relationship between ΔV_A and ΔV_B can be expressed as

$$\frac{\Delta V_B}{\Delta V_A} = \frac{g_{m2}}{g_{m1}} = \left(\frac{2I_d \cdot C_{\rm OX2} \cdot \mu_2 \cdot \frac{W_2}{L_2}}{2I_d \cdot C_{\rm OX1} \cdot \mu_1 \cdot \frac{W_1}{L_1}}\right)^{\frac{1}{2}}. \tag{4}$$

As long as T1 and T2 are locally matched, (4) can be simplified as

$$\frac{\Delta V_B}{\Delta V_A} = \left(\frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}}\right)^{\frac{1}{2}}. \tag{5}$$

The ratio of ΔV_B to ΔV_A observed from the theoretical analysis is only dependent upon the geometric size of TFT. At such condition, *W/L* ratio of T1 should be enlarged to allow $\Delta V_B/\Delta V_A$ as small as possible. Thus, the charge injection mechanism cannot directly affect the critical gate voltage so that the proposed SI memory can effectively achieve the accurate reproducing current by optimizing the size of TFT. Therefore, not only the small capacitance is acceptable for the proposed SI memory design, but the response time of the SI memory is also improved by reducing the size of storage capacitance.

III. EXPERIMENT

The prototype of the proposed SI memory has been designed and evaluated by taking advantage of the simulation program Smart-SPICE and the Rensselaer Polytechnic Institute (RPI), Troy, NY, poli-Si TFT model. Table I lists the parameters used in designing the SI memory. Besides, the laser annealing LTPS-TFT technology is used to fabricate the proposed SI memory which is shown in Fig. 2. The dirct measurement of critical gate voltage of SI memory has severe limitation due to the small storage capacitor of 100 fF. The parastic capacitance of measurement probe, usually several picofarad, greatly affects the measurement accuracy of the probed node when the falling rate of the critical voltage is high. An additional unit gain operation amplifier can be used to circumvent the problem and to be a better monitor of critical gate voltage, as schematically shown in Fig. 3. The operation amplier possesses the excellent driving capability to track the input voltage precisely, therefore, suitable for the interface with measurement system. The input current signal with a range of 0.1 to 12 uA is provided by the bias circuit. The pixel-like circuit is designed as an active loading for SI memory. The entire measurement system diagram is shown schematically in Fig. 4.

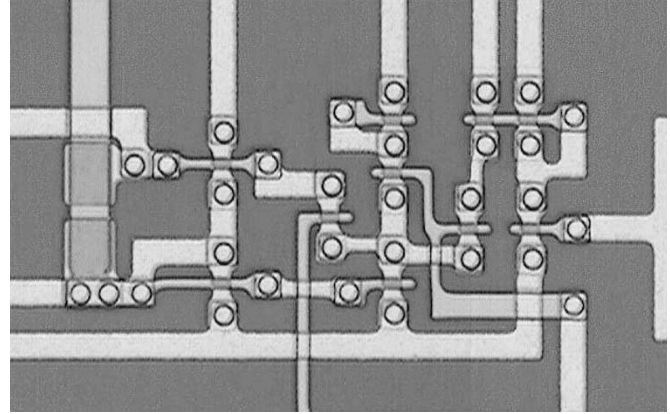

Fig. 2. Photograph of porposed SI memory fabricated by LTPS-TFT process.

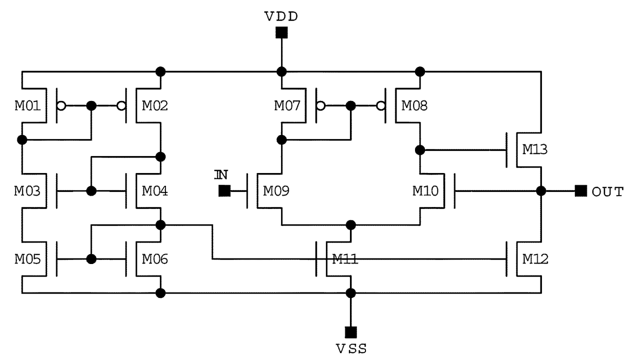

Fig. 3. Schematic diagram of unit gain operation amplifier for measurement of critical gate voltage.

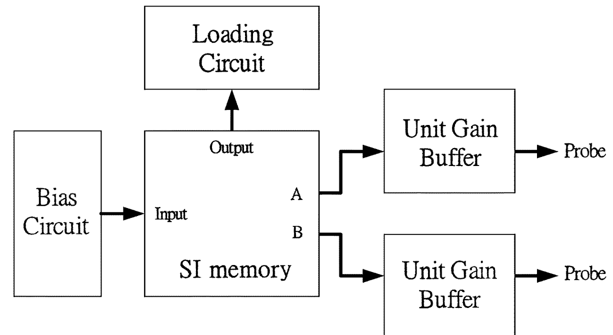

Fig. 4. Diagram of SI memory measurement system.

The critical gate node B isolated from switch T3 in proposed SI memory is not perturbed by charge injection directly, as previously discussed. Furthermore, (5) indicates that the increase of geometric size of T1 is beneficial for reducing the critical gate voltage error without using

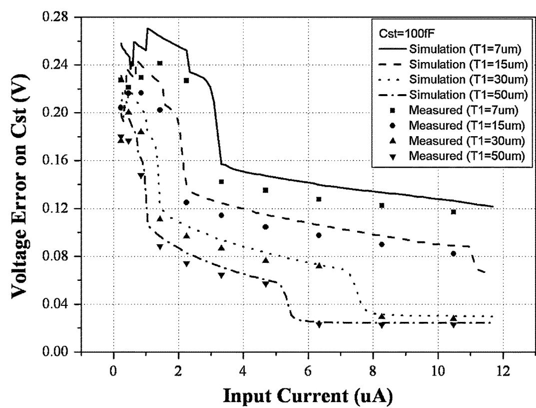

Fig. 5. Voltage error at node B in proposed SI memory with different T1 geometric size.

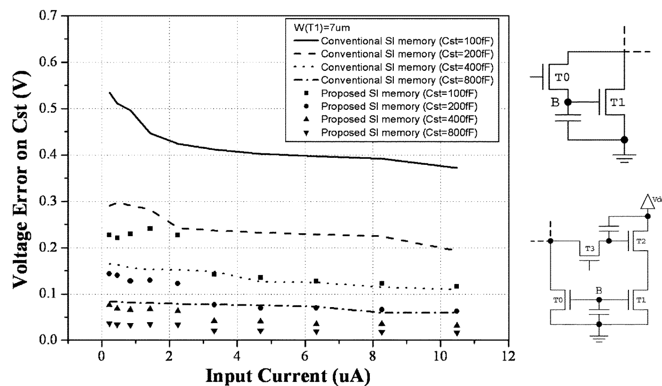

Fig. 7. Measured voltage error at node B in both conventional and proposed SI memory with *W/L* ratio of 7/5.

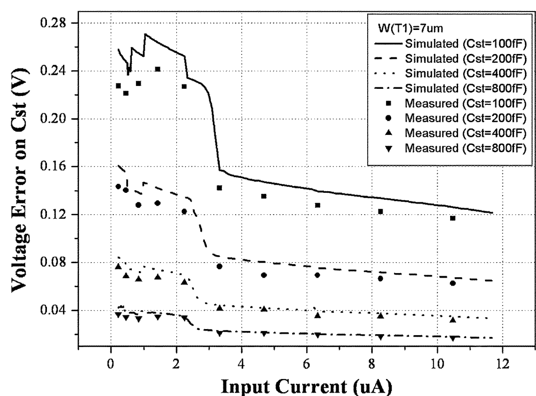

Fig. 6. Voltage error at node B in proposed SI memory with different capacitance.

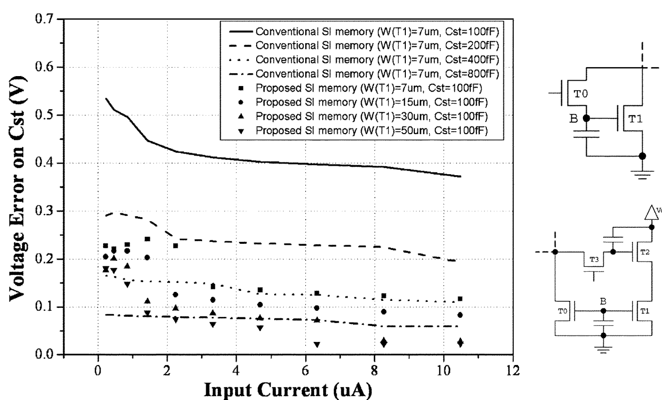

Fig. 8. Measured voltage error at node B in both conventional and proposed SI memory.

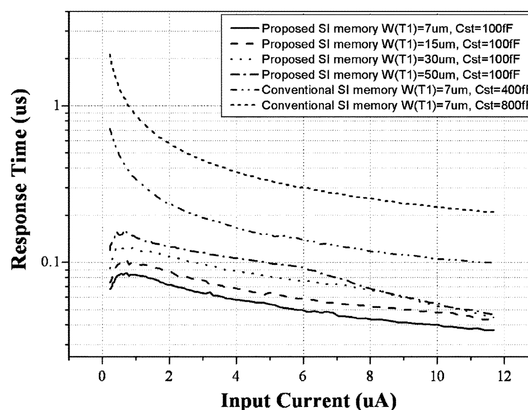

Fig. 9. Simulation results of response time of both SI memory.

large capacitance. The characteristics of voltage error versus input current with different size of T1 were measured and are illustrated in Fig. 5. It is evident that the minor critical gate voltage error is achieved by increasing T1 size from 7 to 50 um. Moreover, large storage capacitor still shows great resistance to charge injection, as confirmed in Fig. 6. However, the critical gate voltage error still increases as the input current becomes smaller, as shown in Figs. 5 and 6. As a result, transistors T1 and T2 driven in subthreshold region of weak current are more sensitive to the charge injection.

The conventional SI memory is also implemented with LTPS-TFT process for the comparison of the influence of charge injection with proposed SI memory. The critical gate voltage error at node B for each SI memory was measured in the same testing condition. Noticeable charge injection casued voltage error can be seen in measurement reults of the conventional SI memory, as shown in Fig. 7. The voltage error in the conventional SI memory is around 0.4 to 0.5 V when using a capacitor of 100 fF. In contrast, the voltage error in proposed SI memory with the same capacitance is less than 0.25 V, almost one-half smaller than that of the conventional SI memory. The capacitor of at least 400 fF is necessarily used to reduce the charge injection induced voltage error less than 0.2 V in the conventional SI memory, therefore, limits the response time of the SI memory.

Critical gate voltage error of less than 0.1 V can be achieved by means of increasing the *W/L* ratio of T1 up to 30/5 in proposed SI memory with capacitance of 100 fF, as plotted in Fig. 8. However, the capacitance of conventional SI memory should be raised to 800 fF so as to accomplish the equivalent voltage error. The above data confirms that the proposed SI memory reveals outstanding resistance to the effect of charge injection even under the usage of the capacitance of 100 fF.

The response time of both conventional and proposed SI memory is evaluated by SPICE program as the isolated critical gate node is difficult to detect directly, as revealed in Fig. 9. The response time of proposed SI memory with capacitance of 100 fF is lower than 0.16 us as the width of T1 varies from 7 to 50 um. The aforementioned results indicate that the capacitance of more than 400 fF is requisite for the approximate voltage error in the conventional SI memory. Thus, the larger capacitance results in the response time of more than 0.7 us, four times higher than that of proposed SI memory.

TABLE II
COMPARISON OF CONVENTIONAL AND PROPOSED SI MEMORY WITH EQUIVALENT VOLTAGE ERROR OF 0.1 V

	Conventional SI memory	Proposed SI memory
Required capacitance (fF)	800	100
W/L of T1 (μm/μm)	7/5	30/5
Response time (μs)	> 0.7	0.13
Layout area (μm^2)	7500	9200
Power consumption at 15k Hz operating freqneucy (mW)	23	68

The experimental results of both conventional SI memory and proposed SI memory have been summarized in Table II. The large capacitance of 800 fF in conventional SI memory merely achieves the equivalent voltage error of 0.1 V as that of proposed SI memory with 100 fF capacitance and *W/L* ratio of 30/5, nevertheless, at the expense of a factor of 4 increase in the response time of proposed SI memory. However, the area consumption of the proposed SI memory is approximately 1.2 times larger that that of the conventional SI memory due to the usage of five TFTs and two capacitors. Besides, the power consumption of proposed SI memory is in a factor of three higher than that of conventional SI memory on account of the constant current conducted in T1 and T2 in proposed SI memory.

IV. CONCLUSION

Design and implementation of new SI memory are described and the measurement results of proposed SI memory fabricated with LTPS-TFT technology are presented. The SI memory operates with only one control signal and has a capability to improve the output current accuracy by suppressing the influence of charge injection. Moreover, fast response time is achieved by the capacitance of small size without sacrificing the output accuracy. Even though the die size and the power consumption of the new SI memory are inferior to those of the conventional SI memory, the features, such as fast response time and high accuracy of output current, favor the applications of the proposed SI memory in driver circuits of current driving active-matrix OLED panels.

REFERENCES

[1] C. C. Wu, S. Theiss, M. H. Lu, J. C. Sturm, and S. Wagner, "Integration of organic LEDs and amorphous Si TFTs onto unbreakable metal foil substrates," in *IEDM Tech. Dig.*, 1996, p. 957.

[2] M. Stewart, R. S. Howell, L. Pires, M. K. Hatalis, W. Howard, and O. Prache, "Polysilicon VGA active matrix OLED displays—Technology and performance," in *IEDM Tech. Dig.*, 1998, p. 871.

[3] T. Shimoda, H. Ohsima, S. Miyashita, M. Kimura, T. Ozawa, I. Yudasaka, S. Kanbe, H. Kobayashi, R. H. Friend, J. H. Burroughes, and C. R. Towns, "High-resolution light emitting polymer display driven by low-temperature polysilicon thin-film transistor with integrated driver," in *Proc. Asia Display Conf.*, 1998, p. 271.

[4] R. M. A. Dawson, Z. Shen, D. A. Furst, S. Connor, J. Hsu, M. G. Kane, R. G. Stewart, A. Ipri, C. N. King, P. J. Green, R. T. Flegal, S. Pearson, W. A. Barrow, E. Dickley, K. Ping, C. W. Tang, S. Van Slyke, F. Chen, J. Shi, J. C. Sturm, and M. H. Lu, "Design of an improved pixel for a polysilicon active-matrix organic LED display," in *SID Tech. Dig.*, 1998, p. 11.

[5] Y. He, R. Hattori, and J. Kanicki, "Improved A-Si:H TFT pixel electrode circuits for active-matrix organic light emitting displays," *IEEE Trans. Electron Devices*, vol. 48, pp. 1322–1325, July 2001.

[6] D. Vallancourt and S. J. Daubert, "Applications of current-copier circuits," in *Analog IC Design: The Current Mode Approach*, C. Toumazou, F. Lidgey, and D. J. Haigh, Eds. Stevenage, U.K.: Peregrinus, 1990, pp. 515–534.

[7] T. Fiez, G. Liang, and D. J. Allstot, "Switched-current design issues," *IEEE J. Solid-State Circuits*, vol. 25, pp. 699–705, Mar. 1990.

[8] R. E. Suares, P. R. Gary, and D. A. Hodges, "All-MOS charge redistribution analog-to-digital conversions techniques—Part II," *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 379–385, Dec. 1975.

Anomalous Poole–Frenkel Mode of Current-Conduction Mechanism in the P-I-N Thin-Film Light-Emitting Diodes

A. Chingsungnoen, P. Kengkan, and W. Tantraporn

***Abstract*—The current density–applied voltage (J–V) characteristics of the p-i-n thin film light-emitting diode (TFLED) were studied. It is found that when the applied voltage is less than the threshold voltage, the current densities of reverse and forward bias are essentially equal. This indicates that the current is limited by the i-layer, which has the highest resistance. In order to study the current-conduction mechanism in the i-layer, numerical approximation in a one-dimensional model is used to calculate the internal distributions of the potential, electric field, and carrier concentration, etc. The theory of anomalous Poole–Frenkel emission gives a calculated result, which agrees with the experimental result. The relationship between the implicated generation rate and radiative recombination rate with electric field is then analyzed. It is found that the electron impact ionization is the primary cause of electron-hole pairs production which upon recombination results in light emission in the i-layer. The current density was calculated by setting appropriate initial conditions for ionization. Radiative recombination rate needed to fit depends on the magnitude of electric field in the i-layer, being slower as the magnitude of electric field increases.**

***Index Terms*—Anomalous Poole–Frenkel emission, current density–applied voltage (J-V) characteristic, p-i-n thin film light-emitting diode (TFLED), Richardson–Schottky conductivity.**

I. INTRODUCTION

The thin film light-emitting diode (TFLED) is one of the optoelectronic devices that has found important applications as a candidate for flat panel display devices. The TFLED converts input electrical energy into output optical radiation in the visible or infrared portion of the spectrum, depending on the quality of semiconductor material. The basic p-i-n TFLED is a p-i-n structure operated under *forward* bias.[1] Although the emission color could be controlled by adjusting the optical gap of the i-layer, the p-i-n TFLEDs made from an amorphous semiconductor have a number of problems that reduce the device light emission efficiency. In these devices, the *symmetric* J–V characteristic in the low–voltage range implies that neither the p-i interface nor the i-n interface proffers the restrictive mechanism on the current flow. The latter is rather controlled by the carrier activation rate within the i-layer. The fact that the barriers differentially are even less resistive at a higher voltage thus cannot account for the current increase in the

Manuscript received December 17, 2003; revised February 25, 2004. This work was supported by the Department of Physics, Khon Kaen University, Khon Kaen, Thailand, under a Grant from the Graduate School. The review of this brief was arranged by Editor L. Lunardi.

A. Chingsungnoen and P. Kengkan are with Department of Physics, Khon Kaen University, Khon Kaen, 40002 Thailand (e-mail: chungsungneon@yahoo.com; 25ex100445@kknet.co.th).

W. Tantraporn is with The Institute for the Promotion of Teaching Science and Technology, Bangkok 10110 (e-mail: wtant@ipst.ac.th).

Digital Object Identifier 10.1109/TED.2004.827364

[1] A bias direction exhibiting a threshold-voltage current jump.

0018-9383/04$20.00 © 2004 IEEE