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A new LVI assisted PSFB DC-DC converter

Ahmet Faruk BAKAN
Department of Electrical Engineering, Yıldız Technical University,
34349, Beşiktaş, İstanbul-TURKEY
e-mail: fbakan@yildiz.edu.tr

Abstract

In this study, a new Phase Shifted Full Bridge (PSFB) Pulse Width Modulated (PWM) isolated dc-dc converter is proposed. In the proposed converter, resonant inductor is replaced with Linear Variable Inductor (LVI) that is controlled by output current. The soft switching operation range is increased and the dependency of ZVS operation on the load current is decreased. The required energy for ZVS operation at low current levels is obtained by means of the high value of the LVI. The value of LVI decreases approximately linearly with increasing current. At high current levels parasitic resonance and duty cycle loss are decreased. By selecting the range of the LVI properly, the necessity of the dead time control between gate drive signals of the IGBTs in the lagging leg is eliminated. A prototype of single phase IGBT-based inverter arc welding machine is implemented by using the proposed converter which operates at 75 kHz switching frequency and 5 kW output power. The experimental results taken from the converter show the feasibility of the proposed method.

Key Words: *DC-DC converters, soft switching, ZVS, PSFB converter, linear variable inductor (LVI)*

1. Introduction

Soft switching techniques are preferred in order to reduce switching losses, current and voltage stresses; consequently, increasing circuit efficiency, power density and decreasing electromagnetic interference in dc-dc converters [1-4]. The Full Bridge (FB) isolated Pulse Width Modulated (PWM) dc-dc converters are widely used in medium-to-high power applications. In these converters, the switching losses and the parasitic resonances between the parasitic capacitance of the power switches and the transformer leakage inductance reach very high values. By means of phase shifting (PS) method, a quasi-resonance between the parasitic capacitance of the power switch and the leakage inductance of the transformer is formed. The energy stored in the leakage inductance is used for the discharging of the parasitic capacitance, and the power switch is turned on with ZVT.

If an IGBT is used as power switch, parasitic capacitance would not be sufficient to provide soft turn off, thus an external snubber capacitor is connected in order to suppress the rate of rise of voltage, and to decrease turn-off losses [5]. ZVS range of the leading leg is wide enough because the required energy for discharging the parallel capacitor is supplied from the load current [6]. At the lagging leg, ZVS is achieved by energy stored in resonant inductor, and ZVS range decreases with increasing value of the external parallel capacitor [5,7].

Most of the recent researches on the PSFB converters are mainly concentrated to solve the problems of the lagging leg [5-18]. By including two additional power switches in primary, the ZVS range of the converter

can be enhanced at the expense of conduction losses [5]. Increasing the leakage inductance of the transformer or adding a large series inductance extends the zero voltage switching (ZVS) range at the lagging leg. On the other hand, this increases the duty cycle loss, the voltage ringing across the output diodes, and the primary conduction losses as well [6, 8]. The energy stored in the magnetizing inductance of the auxiliary transformer can be used to extend the ZVS range [9], but this increases conduction losses. Replacing linear inductor with a saturable inductor extends the ZVS operation range, and reduces duty cycle loss and voltage ringing [10, 11]. However, over-heating of the saturable inductor is a severe problem, and size of magnetic core causes significant increase in the cost [12, 13].

Family of FB converters with additional series coupled inductors has been proposed, which can achieve ZVS from a full load to a no load condition without increasing the conduction loss [9], [10]. However, the voltage unbalance of the transformer at starting up exists in these converters. Furthermore, if the operation duty ratio is large and the leakage inductance of the transformer is very small, the magnetizing inductance of the coupled inductor must be small enough to ensure enough magnetizing current to achieve ZVS. This may result in large conduction losses at light load.

A new ZVS FB converter has been proposed in [14], which can increase ZVS range of the primary switches, and reduce duty-cycle loss. The main idea is to use two power transformers in series. At start up, transformers voltages are unbalanced. In the proposed converter, there are two additional coupled inductors, two clamp diodes, a snubber capacitor, and two rectifier diodes in addition to the normal PSPWM converter components. These additional components increase the complexity and cost of the converter.

In [15], the ZVS operation is achieved over the entire conversion range in the PSPWM converter. But the method is not appropriate for arc welding machines. The proposed converter is suitable for applications where the load resistance is fixed.

In a recent study [16], zero-voltage switching (ZVS) for the leading leg and zero-current switching (ZCS) for the lagging leg switches are achieved in the converter operating at 3kW and 50kHz. But, the proposed topology requires many circuit elements in addition to the PSPWM converter components. A power MOSFET, a capacitor and a free-wheeling diode are used for active energy recovery clamp. Auxiliary circuit is implemented with a transformer, a diode bridge, and two inductors. Besides, a control signal and drive circuit are required for power MOSFET.

In this study, a new method is proposed to improve the ZVS range of the lagging leg. The resonant inductor in the PSFB converter is replaced with Linear Variable Inductor (LVI) which is controlled by output current. The proposed converter has advantages over recently developed PSFB dc-dc converters in terms of duty cycle loss, output voltage ringing, and efficiency. The proposed method does not increase circuit complexity and only an additional magnetic core is required. The soft switching operation range is extended and dependency of ZVS operation on the load current is decreased. At low currents, the required energy for ZVS operation is obtained by means of high value of the LVI. At high currents, parasitic resonances and duty cycle loss are reduced. By selecting the range of the LVI properly, the necessity of the dead time control between gate drive signals of the IGBTs in the lagging leg is eliminated. A prototype of single phase IGBT-based inverter arc welding machine is implemented by using the proposed converter operating at 75 kHz switching frequency with 5 kW output power. The duty cycle loss, which is about 34% in the normal PSFB converter, reduces to about 15% in the proposed LVI assisted PSFB converter, at full output current. The experimental results taken from the converter demonstrate that the proposed method has promising feasibility.

2. Proposed PSFB converter

The proposed PSFB converter is shown in Figure 1. The converter consists of four IGBTs (Q_1-Q_4) with reverse diodes (D_1-D_4), parallel snubber capacitors (C_1-C_4), a high frequency transformer $(Trf1)$, a DC blocking capacitor C_{DC}, a resonant inductor (L_S, LVI), two output rectifier diodes (D_{O1} and D_{O2}), and an output filter L_O. In order to decrease turn off losses of the IGBTs, high valued parallel snubber capacitors are used in the converter. It is important to determine the maximum and minimum values of the LVI in terms of discharge of the snubber capacitors at minimum and maximum output currents. Leading leg transition and lagging leg transition, respectively, occur in one period of PSFB converter. ZVS range of leading leg is wide enough, and the operation of the leading leg is explained in [5,7]. In this study, only lagging leg transition analysis will be given in detail.

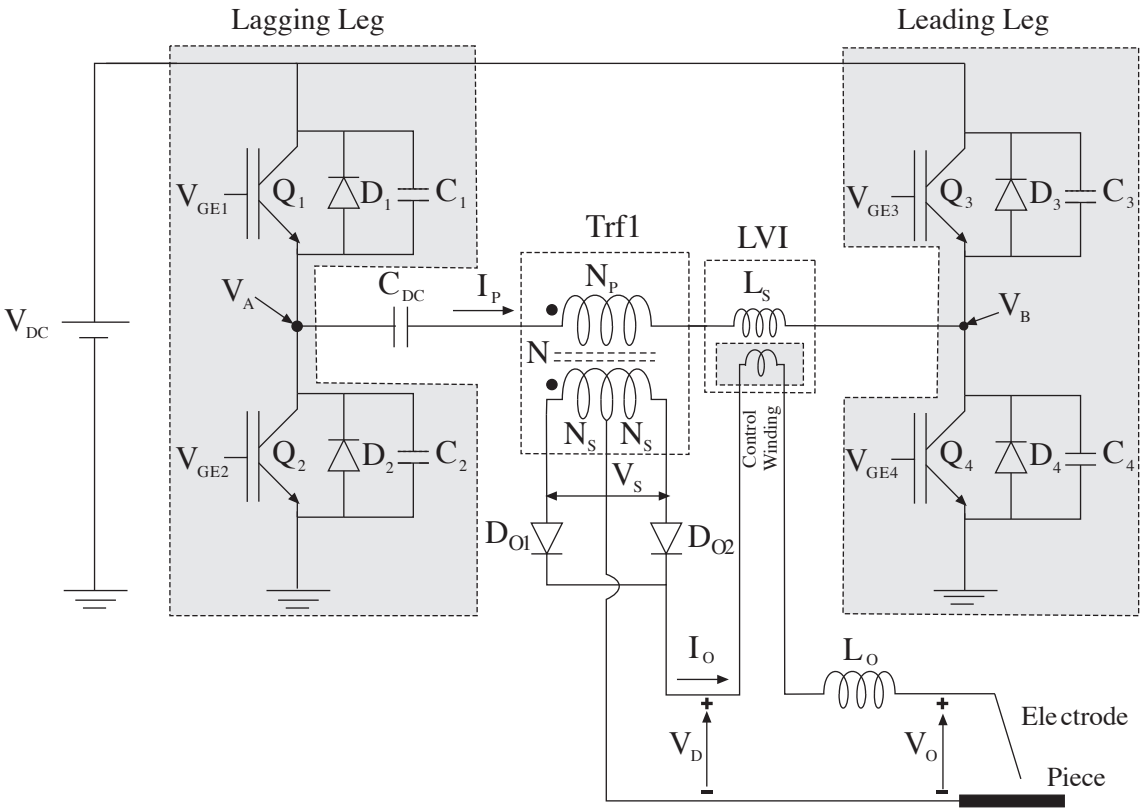

Figure 1. LVI controlled PSFB dc-dc converter for arc welding applications.

The operation waveforms of the PSFB converter are shown in Figure 2. Before $t < t_0$, Q_1 and D_3 are conducting. At $t = t_0$, the drive signal V_{GE1} is removed and lagging leg transition starts. The equivalent circuit for the lagging leg and related waveforms are shown in Figure 3(a). Before $t < t_0$, switch S is closed, $V_{C1} = 0$, $V_{C2} = V_A = V_{DC}$, and $I_L = I_L(0)$. When the switch S is opened at $t = t_0$, the energy of the inductance charges C_1, and discharges C_2. Capacitor currents are given as

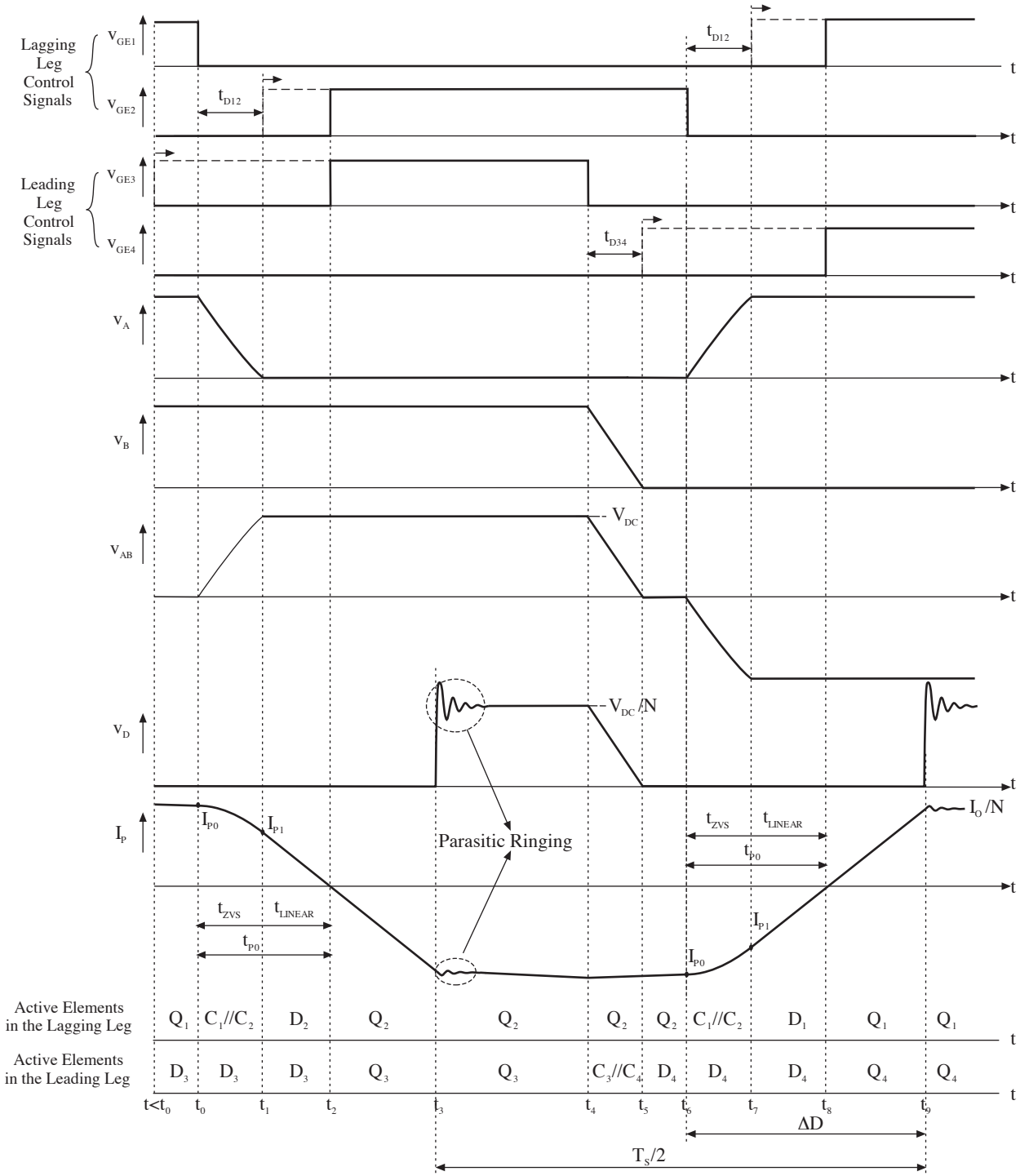

Figure 2. Operation waveforms of the PSFB converter.

$$I_{C1} = C_1 \frac{dV_{C1}}{dt} \tag{1}$$

$$I_{C2} = C_2 \frac{dV_{C2}}{dt} = C_2 \frac{d(V_{DC} - V_{C1})}{dt} = -C_2 \frac{dV_{C1}}{dt}, V_{DC} = \text{constant}. \tag{2}$$

Inductor current is

$$I_L = I_{C1} - I_{C2} = (C_1 + C_2)\frac{dV_{C1}}{dt} = C_P\frac{dV_{C1}}{dt}. \tag{3}$$

The equivalent circuit of Figure 3(a) is given in Figure 3(b). Due to the resonance, the series capacitors can be replaced with an equivalent parallel capacitor and dc voltage supply can be shorted. From Eq.(3), the equivalent parallel capacitor C_P is obtained as

$$C_P = C_1 + C_2. \tag{4}$$

In the series L-C resonant circuit shown in Figure 3(b), the initial inductance current is $I_L(0)$ and initial capacitor voltage $V_{CP}(0) = 0$. Circuit equations can be derived as follows:

$$I_L = I_L(0)\cos(\omega t) \tag{5}$$

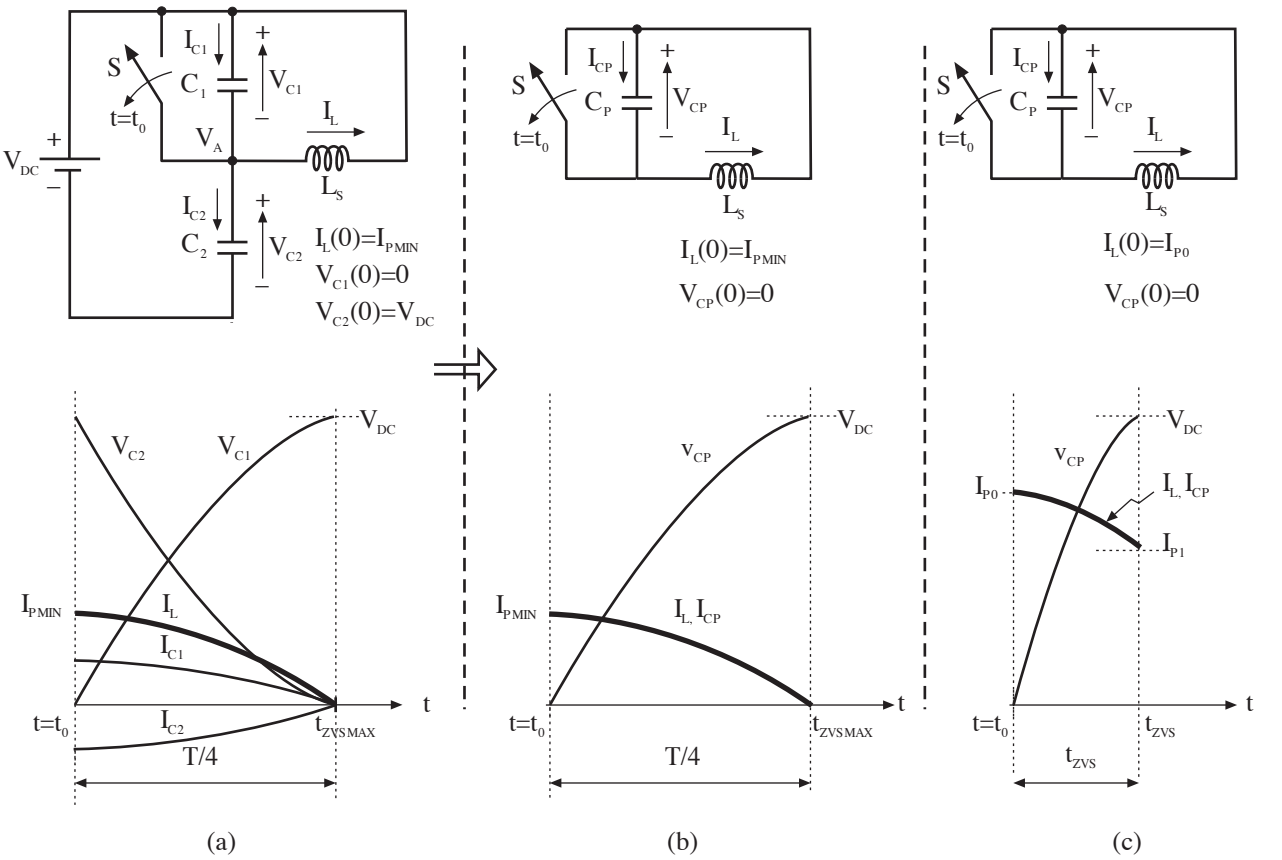

Figure 3. a) Lagging leg transition circuit and waveforms for $I_L(0) = I_{PMIN}$, b) Equivalent circuit and waveforms for $I_L(0) = I_{PMIN}$ and c) Equivalent circuit and waveforms for $I_L(0) = I_{P0}$.

$$V_{CP} = I_L(0)\omega L_S \sin(\omega t) \tag{6}$$

$$\omega = 1/\sqrt{L_S C_P} \tag{7}$$

$$T = 2\pi\sqrt{L_S C_p}. \tag{8}$$

Here, ω is angular frequency, and T is resonance period. For ZVS condition the inductance energy should be high enough to charge the parallel capacitor C_P to V_{DC}.

$$\frac{1}{2}L_S I_P^2 \geq \frac{1}{2}C_P V_{DC}^2 \tag{9}$$

From this energy relation, the minimum current level I_{PMIN} required to provide ZVS is given by

$$I_{PMIN} = V_{DC}\sqrt{\frac{C_p}{L_S}}. \tag{10}$$

For the complete charge/discharge of the parallel capacitor, primary current should be larger than I_{PMIN}. When $I_p = I_{pMIN}$, resonance duration is maximum and capacitor charges to V_{DC} in quarter resonance period as shown in Figure 3(b). Primary current falls to 0 and V_{CP} reaches to V_{DC} at the end of

$$t_{ZVSMAX} = \frac{T}{4} = \frac{\pi}{2}\sqrt{L_S C_P}. \tag{11}$$

If the parallel capacitor is not discharged at the end of t_{ZVSMAX}, reverse resonance occurs and soft switching is lost.

If $I_P > I_{PMIN}$ as shown in Figure 3(c), the parallel capacitor voltage V_{CP} increases from 0 to V_{DC} in t_{ZVS} duration. If the initial inductance current $I_L(0) = I_{P0}$, then t_{ZVS} duration can be derived from (6) as follows:

$$V_{CP} = I_{P0}\omega L_s \sin(\omega t) = V_{DC} \tag{12}$$

$$t = \frac{1}{\omega}\arcsin(\frac{V_{DC}}{I_{P0}\omega L_S}) = t_{ZVS} \tag{13}$$

$$t_{ZVS} = \sqrt{L_S C_P}\arcsin\frac{V_{DC}}{I_{P0}}\sqrt{\frac{C_P}{L_S}} \tag{14}$$

At the end of resonance I_P falls from I_{P0} to I_{P1} and current is commutated to D_2. I_{P1} can be obtained from

$$\frac{1}{2}L_S(I_{P0}^2 - I_{P1}^2) = \frac{1}{2}C_P V_{DC}^2. \tag{15}$$

At $t = t_2$, negative voltage is applied to L_S and current falls to zero linearly in t_{LINEAR} duration.

$$t_{LINEAR} = L_S\frac{I_{P1}}{V_{DC}} \tag{16}$$

Change of the primary current from I_{P0} to 0 takes place in the duration t_{P0} as shown in Figure 2.

$$t_{P0} = t_{ZVS} + t_{LINEAR} \tag{17}$$

At the end of t_{ZVS} duration V_{GE2} should be applied to the IGBT. The dead time t_{D12}, required between Q_1 and Q_2, should provide

$$t_{ZVS} < t_{D12} < t_{P0}. \tag{18}$$

If $t_{D12} > t_{P0}$, current changes direction, reverse resonance starts, and Q_2 turns on with hard switching. Energy of the parallel capacitor is dissipated on the transistor.

Duty cycle loss ΔD is defined as the duration of the change of the primary current from -I_{P0} to $\frac{I_O}{N}$ as shown in Figure 2. In this duration, the rectified output voltage V_D is zero because two rectifier diodes are conducting simultaneously. If it is assumed that $\frac{I_O}{N} \cong I_{P0}$, then duty cycle loss is given as,

$$\Delta D = t_{ZVS} + t_{LINEAR} + t_{LINEAR}\frac{I_{P0}}{I_{P1}}. \tag{19}$$

The percentage of the duty cycle loss $\Delta D(\%)$ is calculated as,

$$\Delta D(\%) = \frac{\Delta D}{T_s/2} = 2f_s\left[t_{ZVS} + t_{LINEAR}(1 + \frac{I_{P0}}{I_{P1}})\right] \tag{20}$$

At high current levels $t_{ZVS} << t_{LINEAR}$, $I_{P0} \cong I_{P1}$, $I_{P0} \cong \frac{I_O}{N}$, and from (19) and (20)

$$\Delta D \cong \frac{2L_S I_O}{V_{DC}N} \tag{21}$$

$$\Delta D(\%) \cong \frac{\Delta D}{T_S/2} = \frac{4f_s L_s I_o}{V_d N} \tag{22}$$

are obtained.

In order to investigate the characteristics of the PSFB converter, the simulation of the converter is realized in MATLAB. In the simulations IGBT is assumed to be an ideal switch. The converter is designed for single phase inverter arc welding machine application with 200 A output current. The characteristics of the proposed converter are obtained with simulation and given in Figure 4. Simulation parameters are selected as V_{DC}=300 V, $C_P = 10nF$, $1\mu H < L_S < 8\mu H$, $f_S = 75\ kHz$, and $0 < I_P < 40\ A$. The value of C_P is high enough to decrease the turn off losses of the IGBTs at nominal current. High values of L_S are not included in the simulations because t_{P0} and duty cycle loss ΔD increase with L_S. Minimum current boundary and minimum dead time for the selected L_S are determined from t_{ZVSMAX} curve. ZVS range and required dead time increase depending on the value of L_S. The minimum dead time is restricted by the turn on and the turn off rates of the IGBTs. Safe dead time is assumed to be t_{D12} >400ns for the selected IGBTs at this power level. Thus, $L_S < 3\mu H$ is not appropriate for minimum dead time requirements. According to Eq. (18), dead time should be smaller than t_{P0}.

For $L_S = 3\mu H$ and $L_S = 8\mu H$, the waveforms of t_{ZVS}, t_{LINEAR} and t_{P0} versus primary current are shown in Figure 5. Dead time should remain in the area between t_{P0} and t_{ZVS} curves. In case $L_S = 3\mu H$, ZVS starts at I_{PMIN}=17.3 A, and dead time t_{D12} should be 272 ns. If t_{D12} is selected as 400 ns, soft switching starts from I_P = 35.7 A (Point A). Small values of L_S is not able to provide dead time requirements and it narrows the soft switching range. In case $L_S = 8\mu H$, ZVS starts at I_{PMIN}=10.6, and dead time should be 445 ns. The minimum dead time provides safe dead time limit t_{D12} >400. If t_{D12} is selected as 400 ns, soft switching below 10.73 A does not occur (Point B). For $L_S = 8\mu H$, t_{P0} is $1.15\mu s$ @ 40 A, and duty cycle loss is 34% at $f_S = 75\ kHz$. Large values of L_S increase duty cycle loss and voltage ringing at the output. Parasitic ringing across the rectifier diode occurs when the voltage rises in the secondary of the transformer as shown in Figure 2. Voltage ringing is mainly affected by the resonance inductance L_S, the junction capacitance of the diode, and the diode reverse recovery characteristics. When voltage is applied to the secondary, one of the rectifier diode is reverse biased, and resonance inductance rings with the diode capacitance. Ringing frequency is calculated as,

$$f_{ring} = \frac{1}{2\pi\sqrt{\left(\frac{Ns}{Np}\right)^2 L_S C_D}} \tag{23}$$

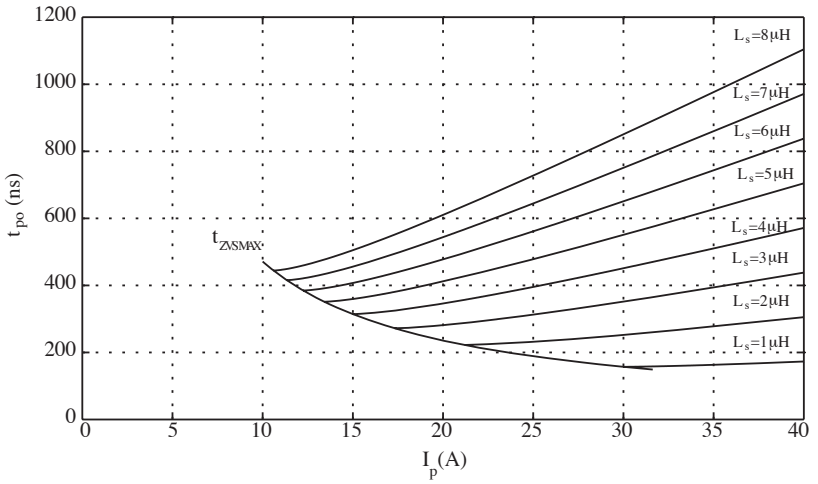

Figure 4. t_{P0} versus I_P for various values of L_S.

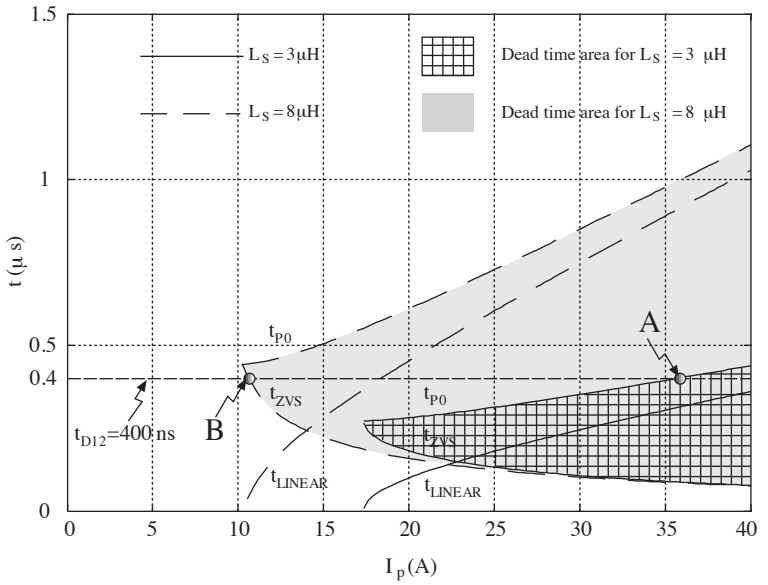

Figure 5. Lagging leg transition durations and dead time areas for $L_S = 3\mu H$ and $L_S = 8\mu H$.

where C_D is the equivalent capacitance of the rectifying diode. Large value of L_S causes ringing at lower frequency, as well as higher diode voltage stress, higher snubber loss, and higher switching noise [6,8,17,18]. Secondary side ringing problems can be solved by using passive snubber, active snubber, or saturable inductor. In this work, saturable inductances are used in series with rectifier diodes to suppress the ringing voltage at the output.

Characteristics of the proposed converter are obtained with simulation and given in Figure 6. Simulation parameters are selected as V_{DC}=300 V, C_P=10 nF, and $0 < I_P < 40\ A$. It is assumed that L_S(LVI) is

changed as shown in Figure 6(a), depending on the output current ($I_P = I_O/N$). With proper selection of minimum and maximum values of LVI, nearly constant dead time in the converter is achieved, and duty cycle loss is not increased with output current. It is seen that t_{P0} is nearly constant in Figure 6(b). Compared to Figure 5 ($L_S = 8\mu H$), duty cycle loss decreases from 34% to 15% at $f_S = 75\ kHz$, at full output current ($I_P = 40A$). As switching frequency increases, the improvement will be more distinguishable.

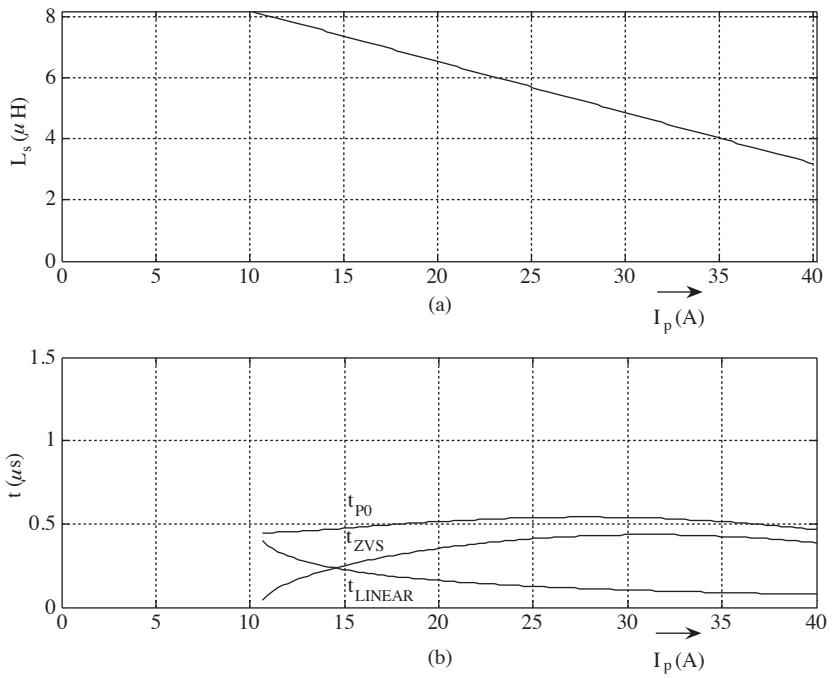

Figure 6. (a) Theoretical variation of LVI, and (b) Lagging leg transition durations for theoretical variation of LVI.

3. Experimental results

To implement the LVI characteristics proposed in Figure 6(a), two identical cores (inductors) are connected electrically in series. These cores are not magnetically coupled. The parameters of the cores are given in Table 1. The basic structure of the implemented LVI is shown in Figure 7. A DC control current generates a DC bias field in both cores, and shifts the operation point into saturation. Without any control current in the control winding, the inductance of the LVI turns out to be maximum. Maximum inductance value of the LVI is obtained with appropriate number of primary turns. Next, the number of control winding turns is adjusted experimentally until the required inductance characteristic is obtained. Φ_{AC1} and Φ_{AC2} do not induce AC voltage in the control winding owing to phase shift of 180^o. In order to saturate ferrite cores over the wide range of control current, a small air gap can be inserted for inductance optimization. Otherwise very large cores may be necessary for LVI design. Increasing air gap too much is not recommended, because the core B-H characteristic becomes approximately linear and required inductance variation characteristic with control current can not be obtained. Control winding current of the LVI is the dc output current of the converter. The current flowing through L_S is the AC primary current.

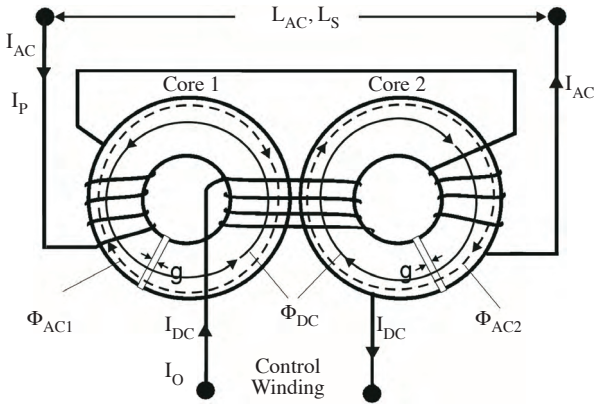

Figure 7. Basic structure of the LVI.

Table 1. Core properties used in LVI prototype.

l	Magnetic length	19.2 cm
A	Core area	4.34 cm^2
μ	Core permeability	1290

The inductance of the implemented LVI is measured depending on the control current as shown in Figure 8(a). The control current is adjusted between 0 - 200 A and this corresponds to the change of I_P between 0 and 40 A. The inductance of the implemented LVI prototype decreases with increasing control current. Lagging leg transition durations are obtained with simulation for the implemented LVI, and given in Figure 8(b).

The developed LVI is replaced with resonant inductor in the PSFB converter. Design specifications and PSFB converter parameters are given in Table 2. The control of the converter is implemented with UC3879.

In order to analyze the output current response of the PSPWM converter, simulations are realized in MATLAB for the implemented LVI, and for $L_S = 1\mu H$ and $L_S = 10\mu H$. Output current reference is set at $I_{ref} = 140A$. Output current is compared with reference current, and duty cycle is changed with PI controller depending on the current error. PI parameters are selected as $K_P = 1.1$ and $K_I = 0.6$ for sampling frequency $f_S = 75kHz$. From the simulated output current responses shown in Figure 9, the output current settles to the reference current in about 100 μs, and relative ripple in the output current is quite low ($\Delta I_O = 7\%$) because of high frequency switching. Overshoot in the output current in LVI assisted PSPWM converter is approximately 25%. Overshoot increases with decreasing L_S, and it is minimum for $L_S = 10\mu H$. The overshoot is also dependent on K_P and K_I coefficients. In the steady state, the duty cycle is 71%, 57% and 45% for $L_S = 10\mu H$, LVI, $L_S = 1\mu H$ respectively. $L_S = 1\mu H$ is shown for comparison purpose, it is not appropriate for implementation. It is concluded that use of LVI does not cause control instability in the PSFB converter, and control design is similar to that in normal PSPWM converter.

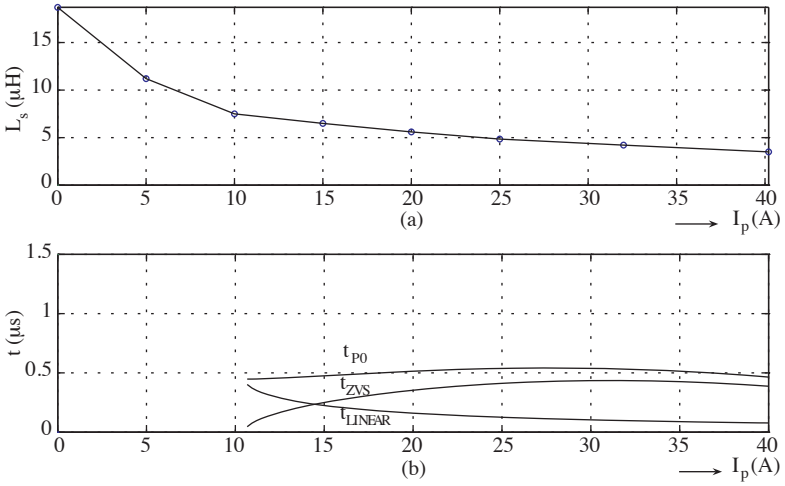

Figure 8. (a) Experimental variation of LVI, and (b) Lagging leg transition durations obtained for experimental variation of LVI.

Table 2. Design specifications and parameters of LVI assisted PSFB converter.

Item	Symbol	Value
Input voltage	V_{DC}	300V
Switching frequency	f_S	75kHz
Dead time	$t_{D12}, \quad t_{D34}$	400ns
IGBTs	$S_1(Q_1 + D_1) - S_4$	IXGH60N60C2D1
Output diodes	$D_{O1} - D_{O2}$	DSEI 2x121-02A
Snubber capacitors	$C_1 - C_4$	5nF-630V
Transformer turns ratio	$N = N_P/N_S$	5:1
Magnetizing inductance	L_M	300μH
Nominal output current	I_O	200A, ($I_P = 40A$)
Output inductor	L_O	10μH

Experimental results taken from the LVI assisted converter are shown in Figures 10-14. The waveforms of primary current I_P, the voltage V_{AB} and gate drive signals of the lagging leg, at minimum primary current providing ZVS, are given in Figure 10. It is seen that ZVS operation starts at approximately I_P=10 A, and dead time between gate drive signals of the lagging leg is 450 ns.

Primary current I_P and the voltage V_{AB} are given in Figures 11, 12 and 13, at output currents 60 A, 130 A and 200 A, respectively. From these figures, it is seen that $t_{P0} = 550\ ns$ and $\Delta D = 1.1\mu s$ approximately. t_{P0} and ΔD are nearly constant at different output currents, due to the decrease of the value of the LVI with increasing output current.

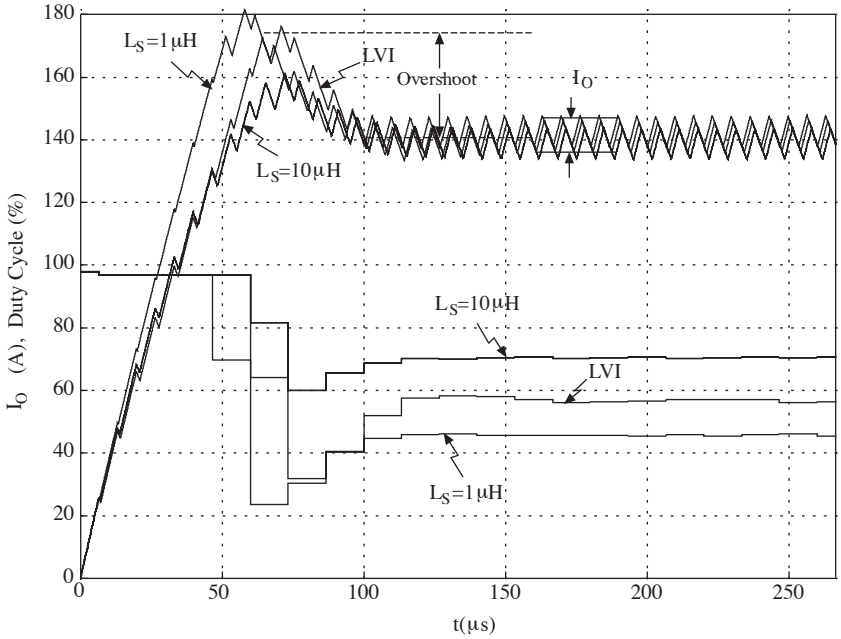

Figure 9. Output current responses and duty cycle waveforms in the PSFB converter for $L_S = 1\mu H$, LVI and $L_S = 10\mu H(I_{ref}$=140A).

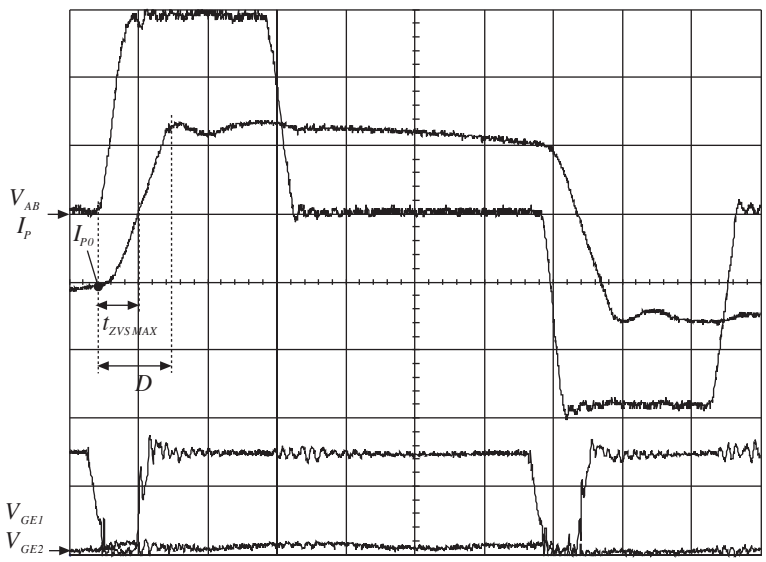

Figure 10. Experimental waveforms of $V_{AB}(100V/div)$, $I_P(10A/div)$, $V_{GEA}(10V/div)$ and $V_{GEB}(10V/div)$ at minimum ZVS boundary (1 μs/div).

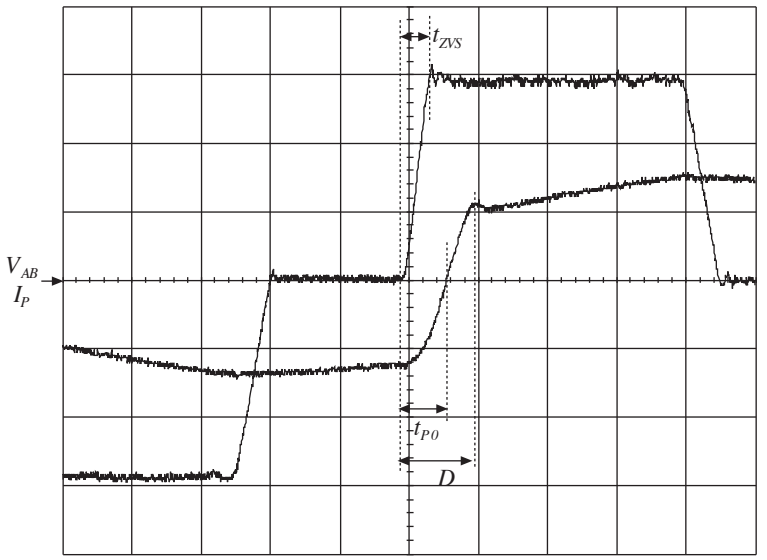

Figure 11. Experimental waveforms of I_P and V_{AB} for $I_o =$ 60 A from LVI assisted converter with 100 V/div, 10 A/div and 1 μs/div scales.

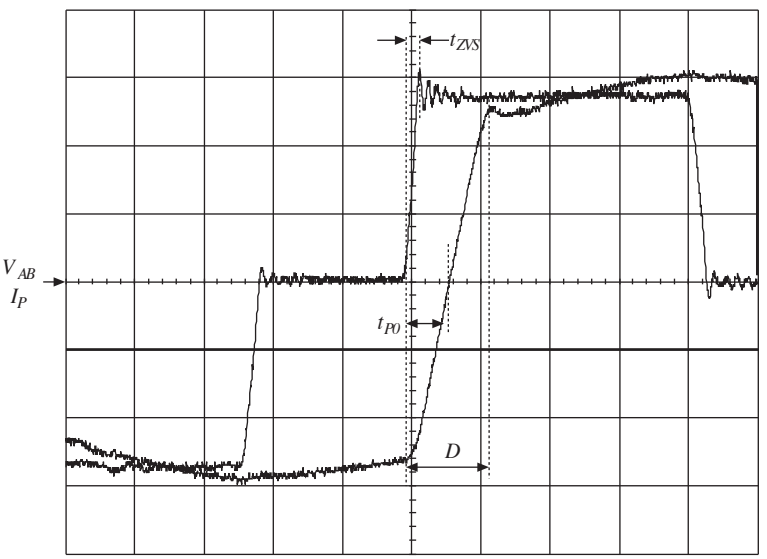

Figure 12. Experimental waveforms of I_P and V_{AB} for $I_O =$ 130 A from LVI assisted converter with 100 V/div, 10 A/div and 1 μs/div scales.

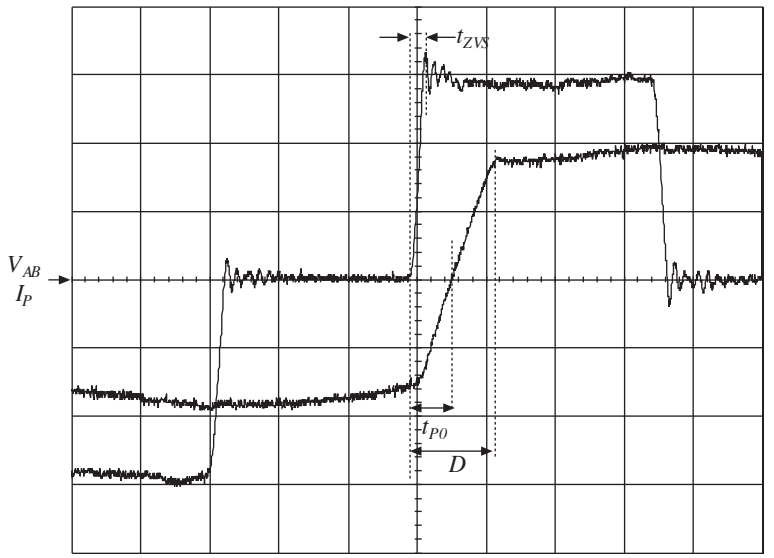

Figure 13. Experimental waveforms of I_P and V_{AB} for $I_O =$ 200 A from LVI assisted converter with 100 V/div, 25 A/div and 1 μs/div scales.

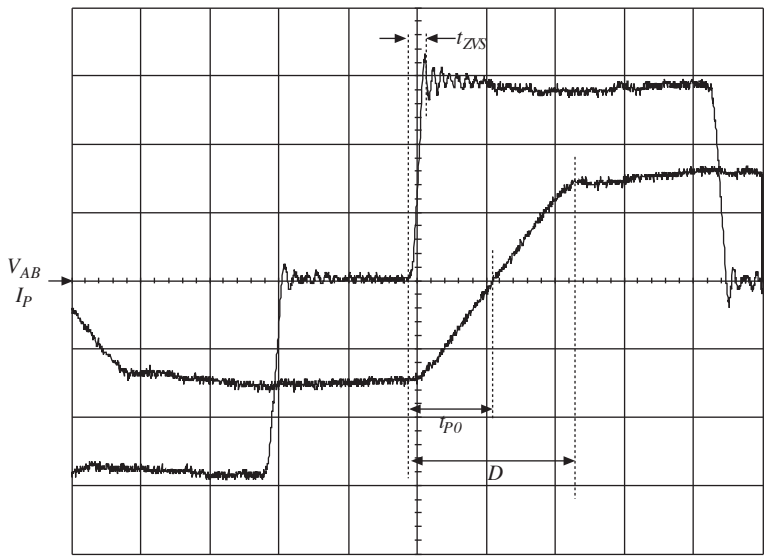

Figure 14. Experimental waveforms of I_P and V_{AB} for $I_O =$ 200 A from normal PSFB converter with $L_S = 8\mu$H. Scales are 100 V/div, 25 A/div and 1 μs/div.

Waveforms of the normal PSFB converter with $L_S = 8\ \mu H$ are given in Figure 14. It is seen that primary current changes its direction in 2.5 μs at nominal current. According to equation (22), the duty cycle loss, which is about 34% in the normal PSFB converter, reduces to about 15% in the proposed LVI assisted PSFB converter, at full output current. Furthermore, output voltage ringing is quite low in the proposed LVI assisted PSFB converter because of the reduced energy in the resonant inductor.

4. Conclusions

In this study, a new Phase Shifted Full Bridge (PSFB) pulse width modulated isolated dc-dc converter is proposed to improve the ZVS range of the lagging leg. In the proposed PSFB converter, IGBTs are used instead of MOSFETs due to their low cost and low conduction losses. In order to operate IGBTs at high switching frequencies, turn-off losses are reduced by means of high valued parallel snubber capacitors. The normal PSFB converter is not well suited for IGBTs because of the limited ZVS range of the lagging leg switches. It is required to employ a large resonant inductor to provide ZVS at the lagging leg, and this increases duty cycle loss and parasitic ringing at high currents, and decreases efficiency.

In the proposed converter, the required large resonant inductor is replaced with Linear Variable Inductor (LVI) which is controlled by output current. The soft switching operation range is extended and dependency of ZVS operation on the load current is decreased. At high currents, parasitic resonances and duty cycle loss are reduced. By means of LVI, the necessity of the dead time control between gate drive signals of the IGBTs in the lagging leg is eliminated. This feature is very important for industrial applications. A prototype of single phase IGBT-based inverter arc welding machine is implemented by using the proposed converter operating at 75 kHz switching frequency with 5 kW output power. The duty cycle loss, which is about 34% in the normal PSFB case, reduces to about 15% in the proposed LVI assisted PSFB converter, at full output current. The proposed method does not increase the number of components in the normal PSPWM converter. The control and design principles are similar to the normal PSPWM converter and control is very simple. The resonant inductor can be replaced with LVI by using an additional core and a control winding in series with the output inductor. But, the size of the implemented LVI is larger than normal resonant inductor, and it is required to make optimization to reduce the size of the LVI. The experimental results taken from the converter demonstrate that the proposed method has promising feasibility in high-power applications where IGBTs are preferred as the power switches.

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