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Micro- and nanostructurization of surfaces – techniques and applications

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In the paper some surface structurization methods are presented. Wet and/or dry etching, and thermal oxidation process have been used to form arrays of gated and non-gated sharp silicon microtips on a silicon wafer. A transfer mold technique (mold) has been applied to produce arrays of silicon carbide (SiC) microtips located on a glass wafer. The surface of the fabricated arrays has been also modificated by thin film metal layers and carbon nanotubes. Current-voltage characteristics of electron sources with a cold cathode build on the base of microtips arrays are presented. A new application of silicon microtips arrays for biochemistry is shown. The process of electrochemical etching of silicon has been used to form porous silicon and porous silicon dioxide layers. Applications of the porous layers for chemical and biochemical analyses are presented. Microstructurized surfaces modificated by carbon nanotubes have been used to improve the field emission characteristics of electron sources, and to obtain a miniature light source.

Keywords: silicon microtips, SiC microtips, porous silicon, transfer mold technique, field emission, carbon nanotubes.

1. Introduction

Micro- and nanostructurization of dielectric, metallic and semiconductor surfaces is used for a modification of such surface properties as topography, roughness, light reflectivity, chemical activity, and biocompability. These features have a potential use in many branches of science and technology, especially in electronics, medicine, chemistry and biochemistry. It is also possible to form surfaces with many micro- and nanostructures, which can be applied in miniaturized microfluidics devices.

Thanks to the quick development of microelectronics and microengineering techniques micro- and nanostructurization of materials surfaces has become possible [1]. Dry and wet etching methods provide new types of medical application, *e.g.*, microfabrication of microneedle arrays for measurements of biopotentials and transdermal delivery of drugs in a non-painful manner (Fig. 1**a**) [2]. The mechanical, chemical and morphological characteristics of materials are crucial in the case of

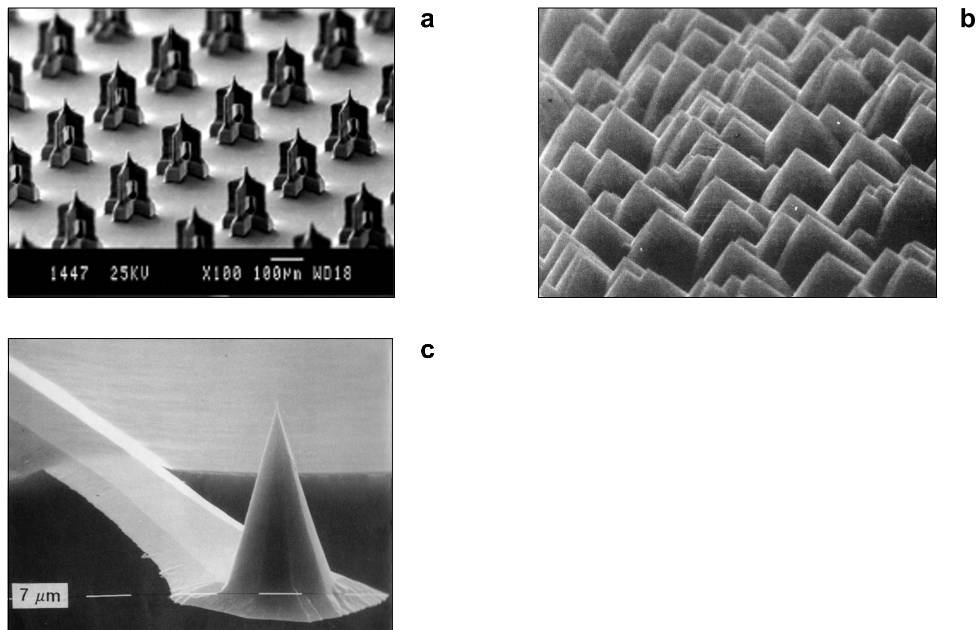

Fig. 1. Structurized silicon surfaces: **a** – microneedles array formed by deep dry etching [2], **b** – silicon pyramids 10 μm high, formed by wet etching for a solar cell [4], **c** – silicon tip formed by wet etching for scanning atomic force microscopy [5].

resulting tissue response and implant durability. It has been stated that the technique of ion sputtering can modify the surface of biocompatible materials by enhancing cells attachment to the implanted material [3].

A standard technique for fabricating solar cells on silicon wafers uses silicon (Si) wafers with textured surfaces [4]. Thus surface texturization is used to minimize reflection and improve the efficiency of cells, with targets aiming towards the currently accepted theoretical limit of about 30%. Wet anisotropic etching along the faces of the crystal planes can texture the surface of crystalline silicon uniformly (Fig. 1**b**).

Surface structurization is also applied in microelectromechanical systems (MEMS). A sharp wet etched silicon tip attached to a cantilever-like spring is used as a probe for scanning atomic force microscopy [5], see Fig. 1**c**. Intentionally modified surfaces are used in new devices with quantum structures, permeable membranes and in photoluminescent and electroluminescent devices [6]. Surface roughening is very effective way of enlarging the intensity of light radiated from semiconductor light emitting diodes. Surface structurization of SiC and Ga-containing semiconductors (Fig. 2) has been realized by dry etching in high-frequency reactive plasmas [7].

Electrochemical etching of monocrystalline silicon has been used as a structurization technique to obtain micro-, meso- or macro-porous surfaces [8]. Recently, porous silicon and porous silicon dioxide layers have been used in micro total analysis systems (μ-TAS) for modification of chemical and electrical properties of surface

microchannels for gas and/or liquid flow (Fig. 3). A porous silicon dioxide layer was fabricated to form electrically insulated microchannels in silicon [9]. Silicon pillars covered with porous layer have been used to increase of gas-liquid contacting surface area in a micromixer [10] and surface activity in an enzyme microreactor [11].

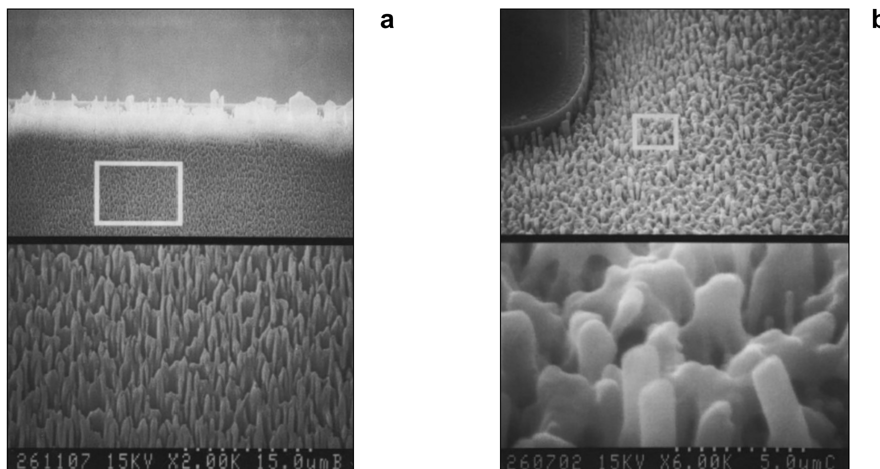

Fig. 2. Structurized semiconductor surfaces: **a** – GaP roughed in reactive plasma containing $Cl_2/O_2/Ar$, **b** – SiC roughed in reactive plasma containing $CF_4/Cl_2/O_2$ [7].

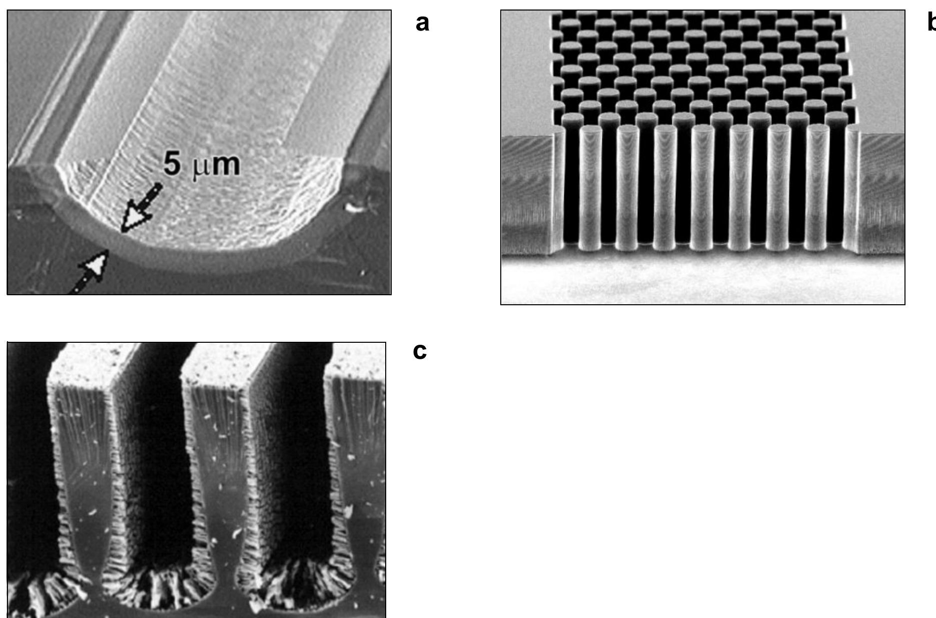

Fig. 3. Fragments of the silicon μ-TAS devices with porous layers: **a** – electrically insulated microchannel [9], **b** – micromixer [10], **c** – enzyme microreactor [11].

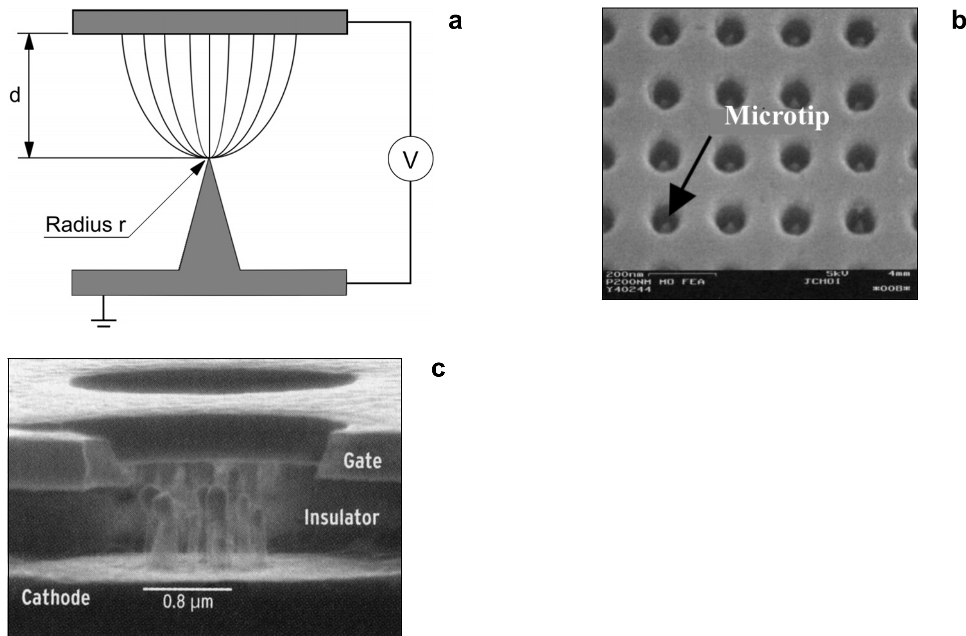

Fig. 4. Illustration of electron field emission from a sharp tip (*r* – radius of a tip summit, *d* – anode–cathode distance) – **a**; Spindt-type microtips array – molybdenum cones surrounded by metallic extraction electrode (gate) [12] – **b**; gated carbon nanotubes cathode [16] – **c**.

Micro- and nanostructurization of surface is used in vacuum microelectronics devices since 1968 [12]. The most representative examples of vacuum microelectronics devices are flat panel displays and miniaturized electron sources for microwaves generators and amplifiers, and spectrometers for space applications [13, 14]. These devices utilize microfabricated field-emission cathodes to obtain electron emission (Fig. 4**a**). Field-emission cathodes contain an array of sharp microtips and are capable of emitting the current in the range of 10–10^4 Acm^{-2} averaged over the total cathode area. The turn-on voltage for electron emission can be very low (from 10 to 200 V) when the sharp microtips are surrounded with an extraction electrode (metal gate) (Fig. 4**b**) [15]. Novel developed cathodes are made from nanomaterials as nanotubes (Fig. 4**c**) [16], nanocomposites or nanostructurized very thin layers [15].

The works on surface structurization started in Faculty of Microsystem Electronics and Photonics of Wrocław University of Technology in 1991 (then Faculty of Electronics). The “Microengineering and Micromechanics Group” was engaged in works on the technology of silicon micromechanical sensors and actuators. Fabrication of 3D silicon microstructures, formation of porous silicon layers, developing of silicon-glass anodic bonding procedure and technology of microtips arrays were the main research challenges.

In this paper some structurization methods and experiment results for fabrication of porous silicon microstructures and arrays of silicon and silicon carbide microtips

have been presented. Wet and/or dry etching, and thermal oxidation process were used to form the arrays of gated and non-gated silicon microtips, and transfer mold technique was used to fabricate the arrays of SiC microtips. To increase emission current, we made array cathodes covered with a thin metal layer, and carbon nanotubes deposited by means the electrophoresis method. Recently, nanostructurized cathodes have been applied to build the miniature light sources with nanocrystalline phosphor. Porous silicon and porous silicon dioxide layers have been used as the elements of bio-samples platforms, for matrix-free mass spectrometry. This new application of structurized surfaces makes possible the identification of the low-mass peptides.

2. Experiments and results

2.1. Arrays of silicon microtips

Silicon field-emission arrays (FEAs) became an important type of cathodes for vacuum microelectronics devices [17]. FEAs are fabricated mainly by use of the various

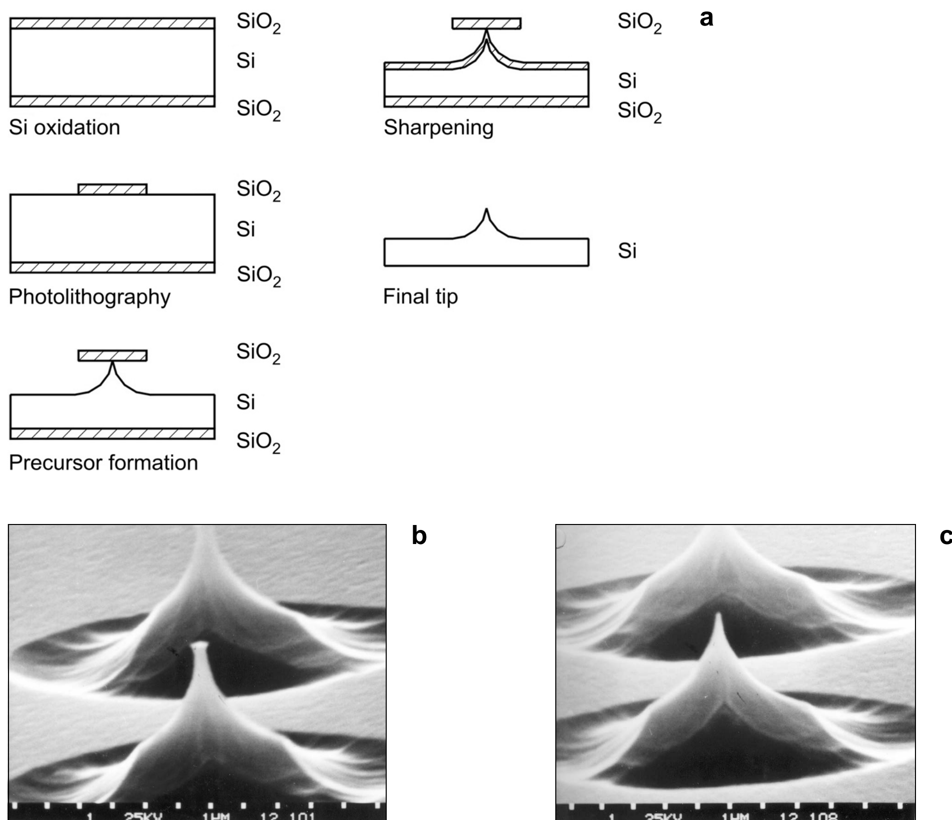

Fig. 5. Step-by-step fabrication process of silicon microtips – **a**; SEM picture of a microtip precursor – **b**; SEM picture of a microtip after sharpening oxidation (Si (100) substrate) – **c**.

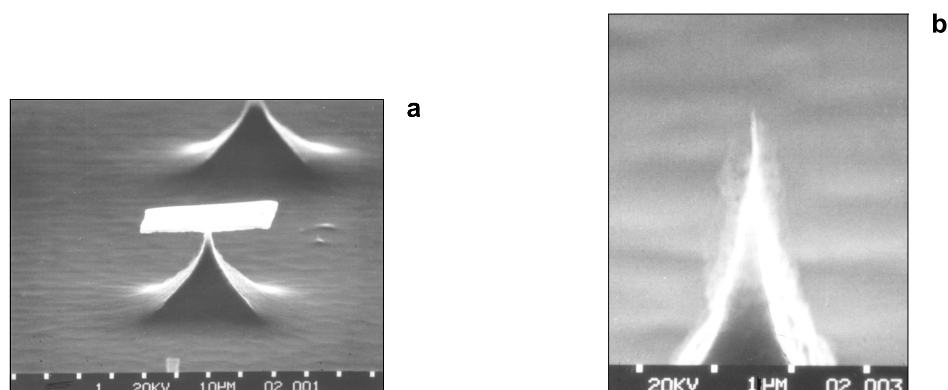

Fig. 6. Silicon microtips fabricated by dry etching: **a** – microtip with Al mask (etching parameters: $p = 2\times10^{-2}$ kPa, SF_6 = 12 sccm, P_{RF} = 150 W; Si (100); GIR-300 Alcatel), **b** – summit of a microtip after Al mask removing [20].

deposition techniques, wet or dry anisotropic or isotropic silicon etching and transfer mold technique.

The step-by-step procedure of silicon surface structurization by use of wet etching is presented in Fig. 5**a**. The 3-inch silicon substrates with resistivity 3 Ωcm, (100) and (111)-oriented, were used. First, silicon substrate was wet thermal oxidized (1100 °C, 3 hours) and thermal oxide masks (1 μm thick) were photolitographically patterned. Then, properly shaped silicon precursors were formed by wet isotropic etching in HNO_3:HF:CH_3COOH = 25:3:10 water solution (NHA), Fig. 5**b**.

Next, the process of microtips sharpening was carried out by thermal oxidation of silicon precursors (950 °C, 2.5 h). Due to the Grove–Deal's effect [18], a thicker oxide layer is generated on a flat surface than on a concave or convex surface. As a result, arrays of 3–5 μm high microtips with summit radius less than 10 nm have been fabricated (Fig. 5**c**) [19]. The final results of sharpening process depend on the quality of photolithography and uniformity of etching process for a whole substrate surface.

Structurization of a silicon surface was also studied by use of dry etching method. The processes of silicon plasma etching were carried out in a reactive ion etching device (GIR-300 Alcatel), with SF_6, SF_6/O_2, SF_6/Cl_2 gas mixtures [20]. Microtips were formed by the use of the silicon dioxide or aluminium masks, and sharpened by applying the thermal oxidation process (Fig. 6).

2.2. Arrays of SiC mold-type microtips

A transfer mold technique offers a unique possibility to move a structurized thin layer from a silicon substrate to a glass wafer. This method allows fabricating micro- and nanostructurized surfaces for many materials, for example: diamond, poly-Si, TiN, LaB_6, [21, 22].

The arrays of microtips made from SiC have been produced for the first time by use of the mold technique [23]. "Negative" replicas of microtips were anisotropically, wet etched in alkaline solution (10 M KOH), in (100) oriented, monocrystalline silicon substrate (Fig. 7**a**). Reversed pyramid-like cavities were filled with an emissive SiC layer, and Si substrate was anodically bonded to Pyrex-like glass wafer. Finally, an unnecessary silicon substrate was removed by wet anisotropic etching. SiC FEAs have been fabricated in two versions: as non-gated arrays (Fig. 7**b**) and as gated arrays (Fig. 7**c**). In the latter case, onto an insulating SiO_2 layer, covering SiC pyramids, the metallic bi-layer (Cr/Au) was deposited, and micrometer-size windows were opened at the summit of tips by wet or dry etching.

The works on the transfer mold technique for SiC FEAs resulted in a new microstructurization possibility. The stage of thin silicon membrane formation has

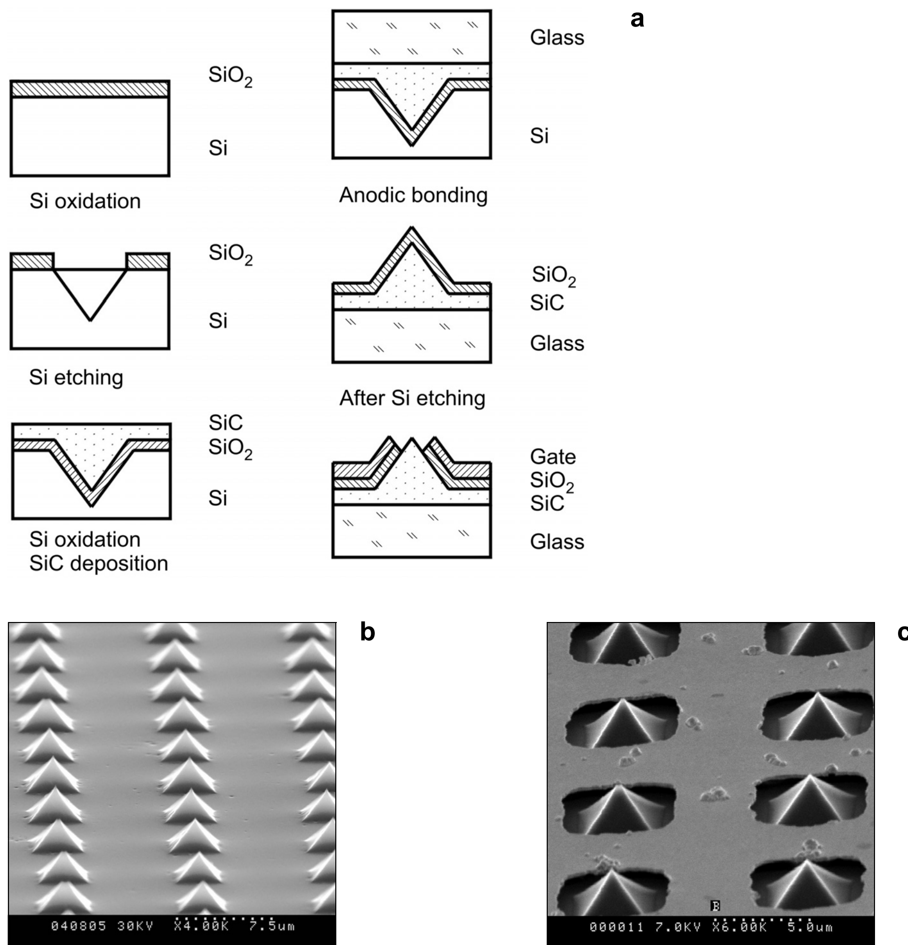

Fig. 7. Step-by-step fabrication process of SiC mold-type microtips – **a**; SEM picture of the non-gated SiC mold-type microtips – **b**, SEM picture of the gated SiC mold-type microtips [23] – **c**.

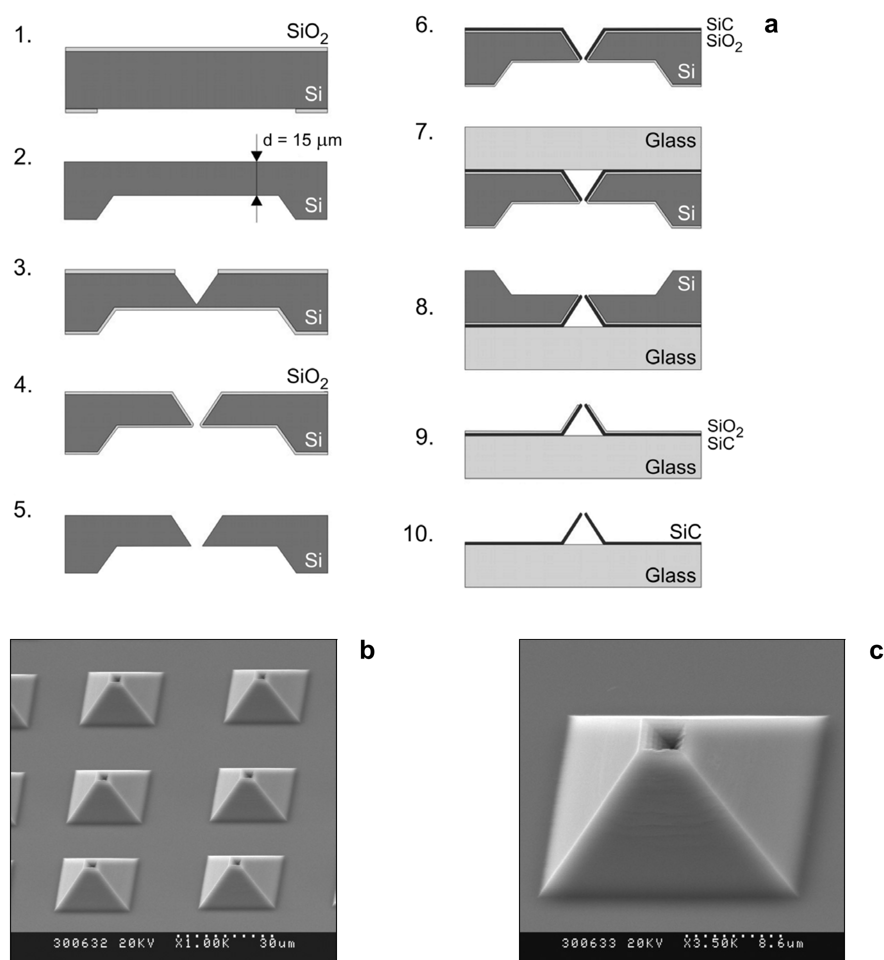

Fig. 8. Array of SiC mold-type microtips with holes at the apex: **a** – step-by-step fabrication process, **b** – SEM picture of the array, **c** – SEM picture of one tip with a crater-like nanometer-sized hole [24].

been introduced to the step-by-step fabrication process (Fig. 8**a**). This micromechanical procedure allowed fabricating an array of pyramid-like cavities, each with a micrometer-sized hole at the bottom. Next, SiC layer has been deposited, and microholes (2×1 μm^2) have been transformed on crater-like nanoholes (100×260 nm^2) in the middle of the tip apex (Figs. 8**b** and 8**c**) [24].

2.3. Porous silicon and porous silicon dioxide layers

Porous silicon layers were produced by the electrochemical method [25]. The 3-inch silicon wafers n- and p-type, (111) and (100) crystallographic orientation were

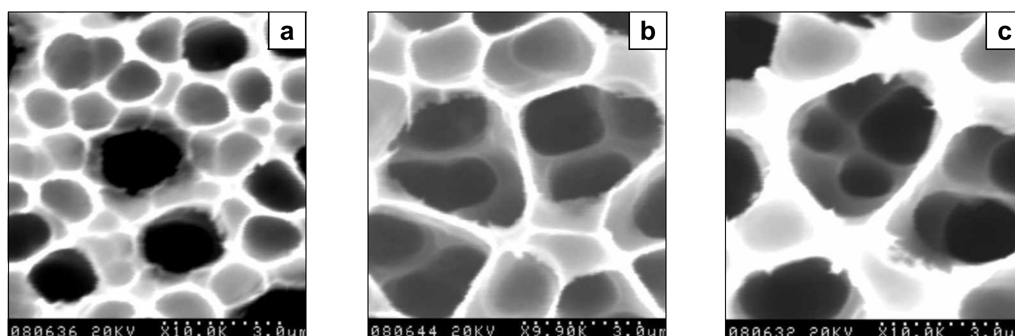

Fig. 9. SEM pictures of porous silicon layers obtained by use of an electrochemical etching for current density 10 mA/cm^2 and etching time: **a** – 6 minutes, **b** – 10 minutes, **c** – 15 minutes [25].

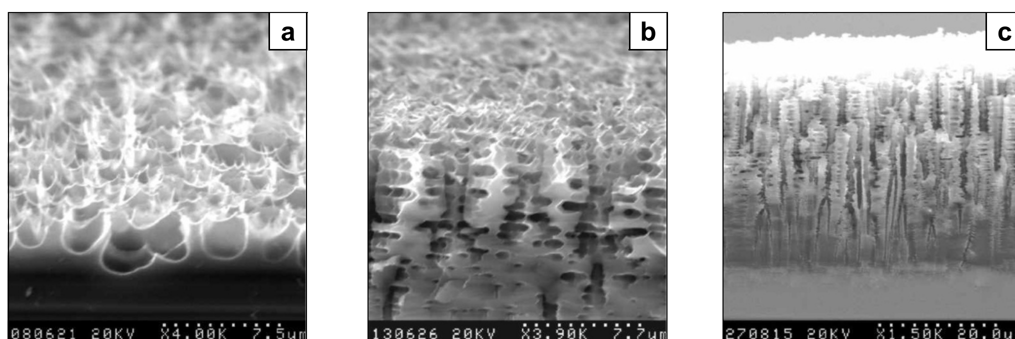

Fig. 10. SEM pictures of porous silicon layers obtained for 6 minutes of electrochemical etching process, and current density: **a** – 30 mA/cm^2, **b** – 70 mA/cm^2, **c** – 110 mA/cm^2 [25].

used. Silicon wafers with Al thin layer deposited onto a back-side were located in an electrochemical cell. Electrochemical etching of silicon has been carried out in the 1:1 (v/v) solution of ethanol (96%) and hydrofluoric acid (40%). Two halogen lamps (12 W, 10 V both) illuminating the front-side of the wafer were used. An adjusting of the etching conditions has controlled thickness and porosity of a porous layer. The diameter and depth of pores increase when the time of etching is longer. Values of diameter/depth of pores equal to 1.24 μm/2.45 μm, 2.12 μm/3.8 μm, 2.26 μm/4.0 μm for 6, 10, and 15 minutes, respectively, were obtained (current density 10 mA/cm^{-2}), (Fig. 9). When the time of silicon etching was fixed (*e.g.*, 6 min) the depth of pores increased when current density was higher (Fig. 10). Porous silicon layers were transformed into porous silicon dioxide layers. This process was carried out carefully by use of wet thermal oxidation method (1050 °C). After oxidation process the layers had smaller pores (Fig. 11).

3. Applications

3.1. Field-emission electron sources

Described silicon surface structurization procedures have been utilized for fabrication of the miniaturized vacuum microelectronics devices. Field-emission electron sources were built on the base of arrays of gated and non-gated microtips made from Si, SiC, and carbon nanotubes.

Arrays of 2500 silicon microtips (1×1 mm^2) covered by platinum/chromium/titanium thin layers were tested as electron sources in diode configuration [26]. Anode was located about 25 μm above the structurized cathode. Test structures were placed in a vacuum apparatus in oil-free atmosphere under vacuum better than 10^{-7} kPa. The resulted current-voltage characteristic is shown in Fig. 12**a**. The maximal current about 300 μA was obtained.

The device with an array of 1715 gated silicon microtips (0.375×0.52 mm^2) was tested for an anode located at 300 μm. For this configuration the low turn-on voltage about 160 V has been obtained (Fig. 12**b**).

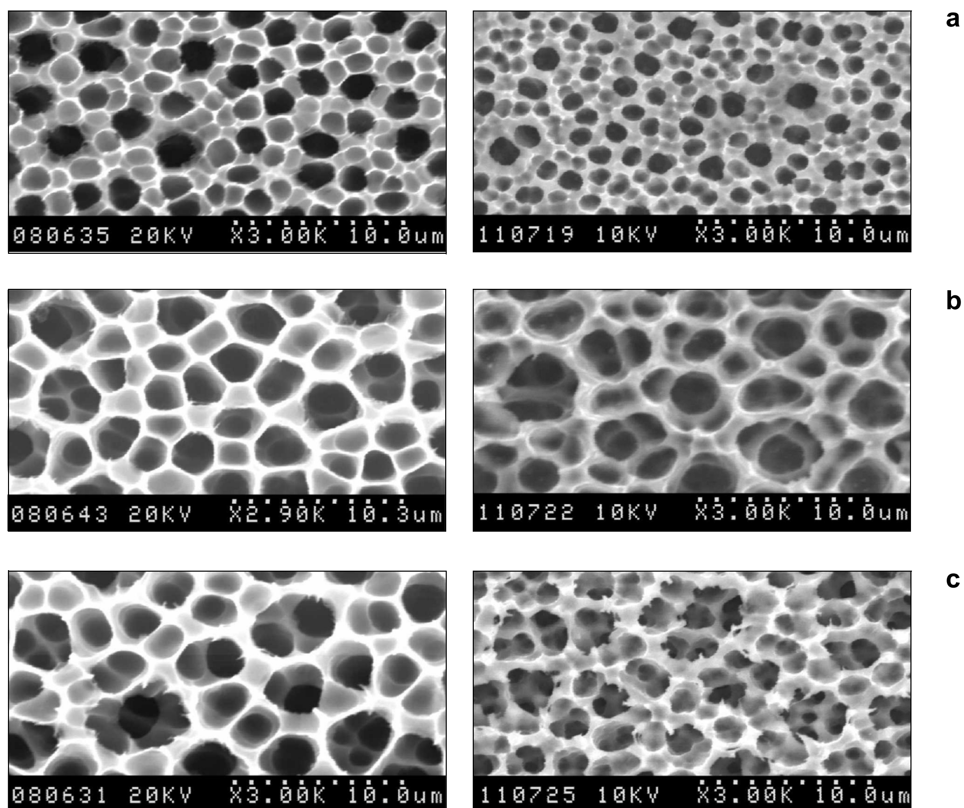

Fig. 11. SEM pictures of porous silicon layers before (left) and after (right) wet oxidation process, obtained for current density 10 mA/cm^2, and etching time: **a** – 6 minutes, **b** – 10 minutes, **c** – 15 minutes [25].

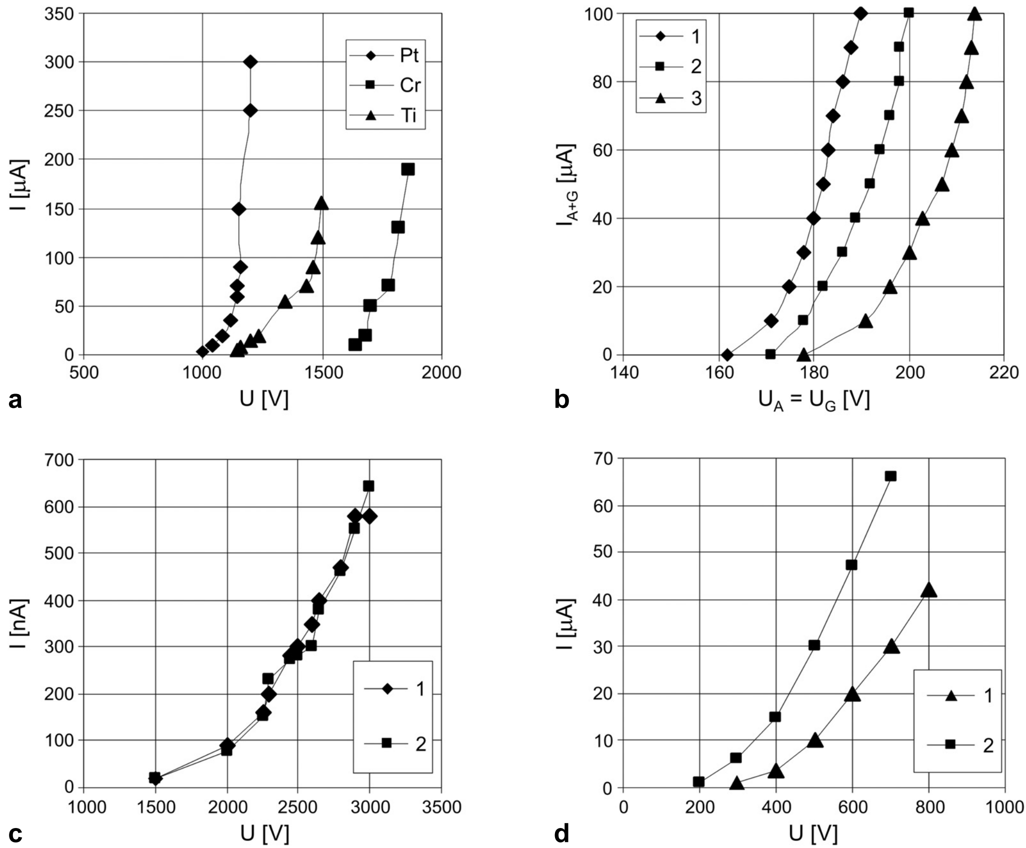

Fig. 12. Field emission characteristics for the electron sources: **a** – arrays of silicon microtips covered with a thin layer of platinum, chromium or titanium [26], **b** – gated array of silicon microtips (3 test structures), **c** – array of SiC mold-type microtips (2 measurements of the same test structure), **d** – array of SiC mold-type microtips covered with multi-walls carbon nanotubes (2 measurements of the same test structure).

Electron field emission from arrays of about 17 thousands of SiC microtips (2×2 mm^2), produced by the transfer mold technique, has been studied in diode configuration [23]. The anode $\Phi = 1$ mm was located 100 µm above a mold-type cathode. For 3 kV the emissive current $I = 600$ nA was obtained (Fig. 12**c**). A significant increase in emissive current has been obtained when SiC mold-type array was covered with carbon nanotubes by use of the electrophoresis method. The turn-on voltage decreased to about 200 V (Fig. 12**d**).

3.2. Field emission light sources

New light sources utilizing the carbon nanotubes and nanocrystalline rare earth doped yttrium aluminium garnet (YAG) phosphors have been recently elaborated [27]. Nanocrystalline YAG:Ce (0.5%) phosphor for an anode screen was obtained by

the modified Pechini method in 900 °C, and electrophoretically deposited onto soda-lime glass covered with a thin ITO (indium tin oxide) layer. Carbon nanotubes for a cold cathode (MWNT, Senyang National Laboratory for Material Science, Senyang, China) were cleaned, suspended in isopropyl alcohol, and deposited by dropping onto a porous silicon substrate. Next, the cathode was distanced 250 μm from anode by a mica spacer. This device was pumped to about 10^{-6} kPa, and light emission characteristics of various voltage supply were measured (Fig. 13). It has been noted that electron field emission was started at about 300 V, and light generation was efficient and uniform for a porous surface covered with carbon nanotubes.

3.3. Chemical and biochemical analyses

The silicon microchannel with a porous surface has been applied in a chromatography microcolumn (Fig. 14**a**) to separate gas mixtures [25]. The microchannel was fabricated in 3-inch, (111) silicon substrates by isotropic etching in $HF:HNO_3 = 1:9$

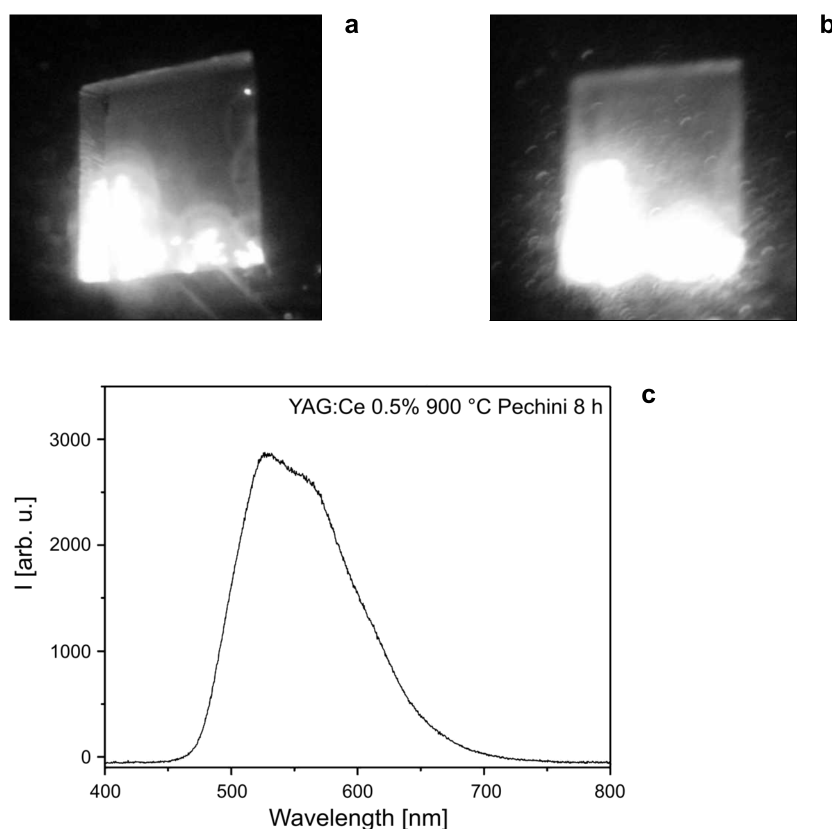

Fig. 13. Miniature light source: **a** – light emitted from YAG:Ce nanocrystalline phosphor deposited on ITO glass anode, anode-cathode voltage supply $U = 400$ V, **b** – light emitted for anode-cathode voltage supply $U = 600$ V, **c** – luminescence spectrum of YAG:Ce 0.5% nanocrystalline phosphor. A field cathode was made from carbon nanotubes deposited onto a porous silicon substrate (1/4 of 3" wafer) [27].

solution. The surface of the microchannel was poroused by electrochemical etching in $HF:C_2H_5OH$ = 1:1 (70 mA/cm^2, 6 minutes). Next, porous silicon was thermally oxidized (1050 °C, 2 minutes, Fig. 14**b**) and a glass cover (Corning 7740) was anodically bonded (450 °C, 1200 V, 70 minutes). The microcolumn with a porous channel 3.7 m long has shown satisfactory separation of gas mixture containing some aromatic hydrocarbons (Fig. 14**c**).

A new porous silicon dioxide platform (DIOSD) for matrix-free desorption/ ionization time-of-flight mass spectrometry has been developed (Fig. 15**a**). Porous

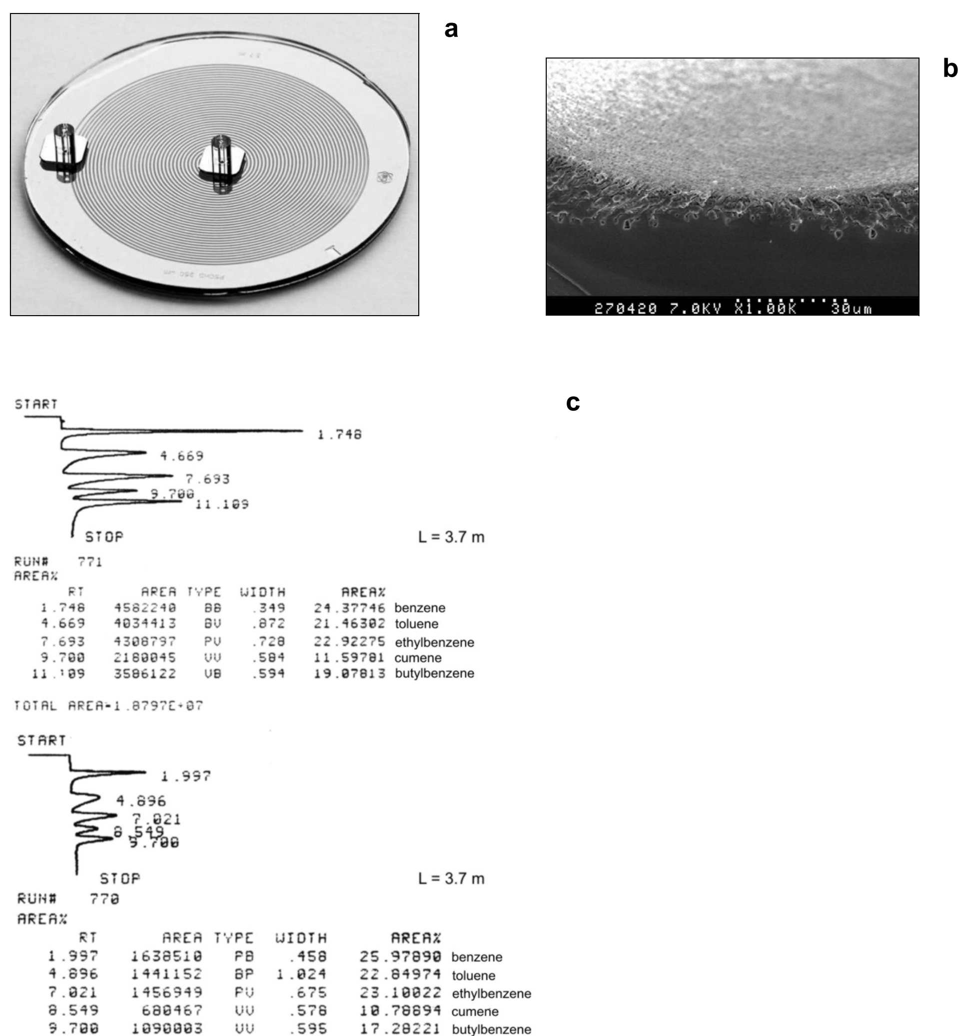

Fig. 14. Porous silicon-glass microcolumn for miniature, integrated chromatograph: **a** – picture of 3-inch, 3.7 m long microcolumn, **b** – SEM picture of porous silicon dioxide on the channel bottom, **c** – chromatograms for aromatic hydrocarbons obtained for a porous (top) and non-porous (bottom) microcolumn for comparison [25].

silicon dioxide spots for bio-samples were fabricated by electrochemical etching of a silicon substrate followed by the high temperature wet oxidation (Fig. 15**b**). It has been shown that porous silicon dioxide spots insure effective laser-induced desorption and ionization of bio-molecules [28]. The noise background signal of DIOSD platform was low, and did not interfere with the measurements (Fig. 15**c**). The 40.79 fmol detectability of tripeptide leucyl–glycyl–glycine was obtained. It turned out that DIOSD might successfully replace the standard matrix-assisted target plate, used in proteomics/peptideomics mass spectrometry, especially for a low-mass biomolecules analysis.

The platform including arrays of silicon microtips (DIOSTA) has been used for laser desorption/ionization of bio-samples for time-of-flight mass spectrometry [29]. Thousands of gated silicon microtips, grouped in spots of varying sizes, were fabricated on a silicon wafer (Fig. 16**a**). Tests made for a dopamine (Fig. 16**b**) have documented clearly that DIOSTA make possible to identify low-mass bio-samples. It seems that different structurized surfaces used in DIOSD and DIOSTA platforms

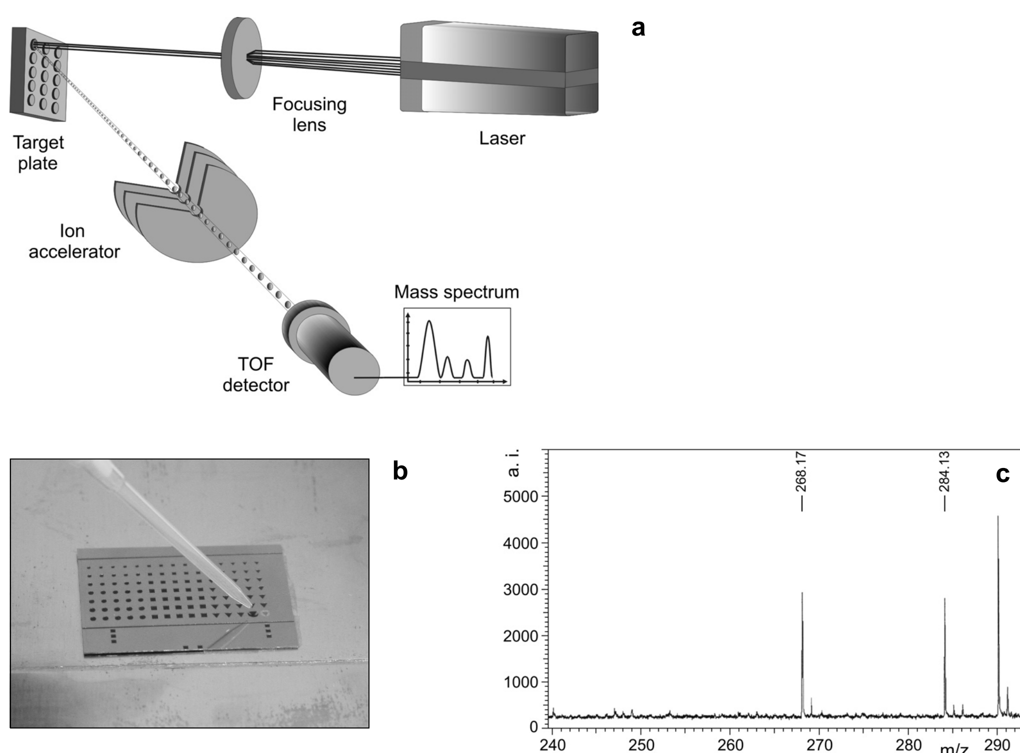

Fig. 15. DIOSD platform – a porous silicon dioxide layer applied in proteomics: **a** – schematic view of MALDI TOF mass spectrometry equipment (Bruker Saxonia), **b** – silicon chip with porous spots, **c** – mass spectrogram of tripeptide leucyl–glycyl–glycine for a dose of 4.079 pmol/spot [28].

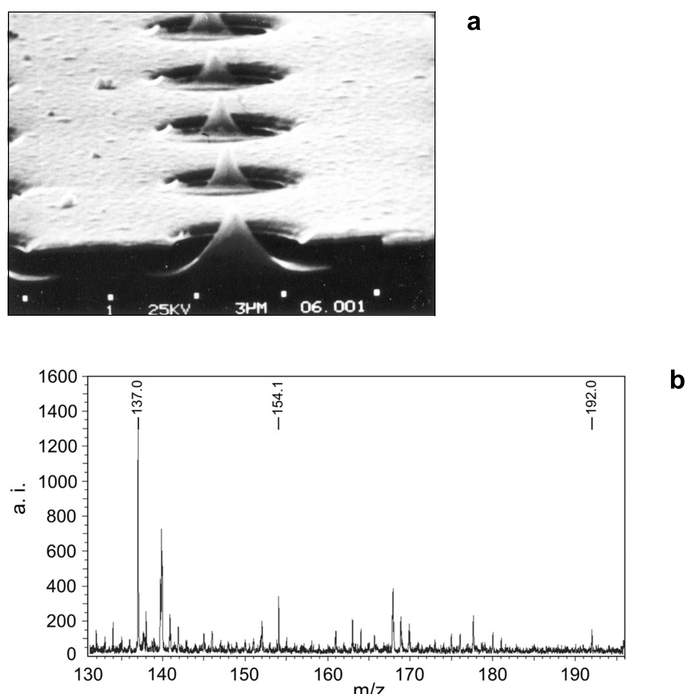

Fig. 16. DIOSTA platform – array of silicon microtips applied in proteomics: **a** – gated silicon microtips array, **b** – mass spectrogram of dopamine for a dose of 65 pmol/spot [29].

can improve and widen identification possibilities of MALDI TOF (matrix assisted laser desorption-ionization time-of-flight) spectrometry.

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