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All-optical 4-bit parity checker design

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A new configuration of all-optical 4-bit parity checker is proposed that incorporates six semiconductor optical amplifiers (SOAs). The proposed 4-bit parity generator is numerically simulated by solving nonlinear coupled equations that explain the cross gain modulation (XGM) effect in individual SOAs. The full design is easy to understand. The outputs can be tested at every step with the help of waveforms. This makes easy error analysis of the circuit. The fault detection and correction can be made comfortably. This design proves that when we reach up to chip level design, the economical circuit is integration capable.

Keywords: optical parity checker, optical logic gates, optical signal processing, semiconductor optical amplifier, cross gain modulation.

1. Introduction

Recently, the success of optical devices such as semiconductor optical amplifiers (SOA) in all-optical signal processing and optical computing has triggered great research interest in them [1–3]. These devices have shown ability to perform direct bit-manipulation in the optical domain which may be used for address recognition, packet header modification and data integrity verification. For data integrity verification, an all-optical parity checker was proposed [4, 5]. As it is well known in electronic digital communication, parity check is one of the most widely used binary manipulations and is attached to a binary word before transmission of the data so that the receiver has the ability to verify the integrity of the recovered digital data. In principle, the optical parity check can be simply generated by using an all-optical XOR gate and a single bit optical delay. In this way, each bit in the binary word is examined in turn in order to generate the overall parity bit at the end of the word. However, it is difficult to obtain a single bit optical delay at present since the all-optical gates themselves generally have a latency larger than that required for single bit delay times. In reference [3], authors have employed a bit-differential design where the binary word to be checked is input several times into an all-optical memory which incorporates the all-optical XOR gate. The memory is configured to have a round trip delay that differs from the repeat time of the input binary word by only one bit. In this way,

the parity of adjacent bits in the input word is accumulated on each circulation around the memory where the XOR function is applied to the input word and the time shifted stored word. The all-optical parity checker of Ref. [3] involves concatenation of two terahertz optical asymmetric demultiplexers (TOADS) at a data rate of 1 Gb/s. Another all-optical parity checker has been simulated that requires a single Mach–Zehnder interferometer (MZI) that allows enhanced and robust operation.

SOAs are prime candidates for use in advanced optical communication functional components. The potential for large-scale integration of SOA technology offers economical, high-performance devices. Using SOAs, various devices can be built with enhanced functionalities as required for future optical communication. SOAs exhibit non-linear properties due to carrier density changes induced by differences in power of the input signal. While these non-linear properties create problems for the use of SOAs as simple linear gain elements, they can be exploited to perform functions that are typically carried out by electronic signal processing circuits. In these applications, the data signal is processed in optical form, rather than first being converted to an electrical signal.

In this paper, we propose a new configuration of the parity checker that is based on cross gain modulation (XGM) in a semiconductor optical amplifier (SOA). The operation speed depends on the carrier recovery lifetime in the active region of the SOA. The typical value for this is around 1 ps, which allows operation up to 100 GHz. This, compared to electrical devices, which are estimated to be limited at 40 GHz due to physical reason, means that XGM can be used for broadband telecommunication application in the future.

SOA-based devices are compact, stable, integration-capable, and potentially independent of polarization and wavelength [4]. Further, they have the advantages of low switching energy and low latency [5]. Further, all-optical logic gates based on semiconductor optical amplifiers (SOAs) are promising because of their power efficiency and their potential for photonic integration [6–12]. In the present paper, based on the nonlinear equations governing XGM in SOA is solved for two input signals that are combined to show a XOR operation. Next, by combining the three XOR gates, an all-optical 4-bit parity checker is realized. The simulated output is shown on MATLAB platform.

2. Simulation method

In our approach, the reference equations are taken from Ref. [13] and different parameters which are taken into consideration are tabulated below in Tab. 1. It is assumed that an input pump, and probe pulses have the same temporal width as well as perfect pulse overlap, and in all of the cases, their powers are set to a ratio of 10:1. Numerical simulations have been undertaken to investigate the amplification of strong picosecond optical pulses in semiconductor optical amplifiers (SOAs), taking into account carrier heating, spectral hole burning, carrier–carrier scattering (CCS) and carrier photon scattering (CPS). The result of interference of two copolarized pulses

T a b l e 1. Parameters used in simulation work.

Parameters	Symbol	Values	Unit
Length of the amplifier	L	450	μm
Small signal gain	G	1.54×10^{-4}	m^{-1}
Carrier lifetime	τ_s	300	ps
Nonlinear gain compression for carrier heating	ε_t	0.13	w^{-1}
Nonlinear gain compression for spectral hole burning	ε_{shb}	0.07	w^{-1}
Traditional linewidth enhancement factor	α	5.0	–
Temperature linewidth enhancement factor	α_T	3.0	–
Linewidth enhancement factor for spectral hole burning	α_{shb}	0,1	–
Time for carrier-carrier scattering	τ_1	50	Fs
Time for carrier photon scattering	τ_h	700	Fs
Carrier depletion coefficient	ε_{cd}	47	w^{-1}

when propagating into SOA, one pump pulse at central frequency ω_1 and the other probe pulse at central frequency ω_0, induces a bit of carrier density pulsation at the frequency detuning $\Omega = \omega_1 - \omega_0$. This results in a generation of a new frequency pulse at $\omega_2 = \omega_0 - \Omega = 2\omega_0 - \omega_1$. The new pulse is a phase conjugate replica of the probe pulses, and can be extracted from the input pulses using an optical filter. Here, $A_j(Z, t)$, $j = 0, 1, 2$, correspond to the slowly varying envelopes of the pump, the probe, and the conjugate pulses, respectively, and $\Omega = \omega_1 - \omega_0$, is the frequency detuning.

$$A_0(L, t) = A_0(0, t)\exp\left[\frac{1}{2}(1 - i\alpha)h\right] \tag{1}$$

where $A_0(0, t)$, is the input pump pulse amplitude at any end of SOA, $A_0(L, t)$, is the input pump pulse amplitude at the length L of SOA, L – length of SOA, t – time. Rest parameters are defined in Tab. 1.

$$A_1(L, t) = A_1(0, t)\exp\left[\frac{1}{2}(1 - i\alpha)h - \eta_{10}\left|A_0(0, t)\right|^2(e^h - 1)\right]\times$$

$$\times \cosh\left[\frac{1}{2}\sqrt{\eta_{02}}\,\eta_{01}^*\left|A_0(0, t)\right|^2(e^h - 1)\right] \tag{2}$$

where $A_1(0, t)$ is the input probe pulse amplitude at any end of SOA, $A_1(L, t)$ is the input probe pulse amplitude at the length L of SOA, L – length of SOA, t – time. Rest parameters are defined in Tab. 1.

$$A_2(L, t) = \frac{A_1^*(L, t)A_0(L, t)}{A_0^*(L, t)}\sqrt{\frac{\eta_{01}}{\eta_{02}^*}}\sinh\left[\frac{1}{2}\sqrt{\eta_{01}}\,\eta_{02}^*\left|A_0(L, t)\right|^2 e^{-h}(e^h - 1)\right] \tag{3}$$

where $A_2(0, t)$ is the input conjugate pulse amplitude at any end of SOA, $A_2(L, t)$ is the input conjugate pulse amplitude at the length L of SOA, L – length of SOA, t – time. Rest parameters are defined in Tab. 1.

$$\eta_{01} = \eta_{01}^{\mathrm{CD}} + \eta_{01}^{\mathrm{CH}} + \eta_{01}^{\mathrm{SHB}} \tag{4}$$

where,

$$\eta_{01}^{\mathrm{CD}} = \varepsilon_{\mathrm{cd}} \frac{1 - i\alpha}{(1 + i\Omega\tau_1) + (1 + i\Omega\tau_s)}$$

$$\eta_{01}^{\mathrm{CH}} = \varepsilon_t \frac{1 - i\alpha_T}{(1 + i\Omega\tau_h) + (1 + i\Omega\tau_1)}$$

$$\eta_{01}^{\mathrm{SHB}} = \varepsilon_{\mathrm{shb}} \frac{1 - i\alpha_{\mathrm{shb}}}{1 + i\Omega\tau_1}$$

The amplification function h and coupling coefficient η_{ij} are defined in [13].

3. Results and discussion

At first, all-optical XOR gate is designed. Basic digital XOR gate and its truth table is shown in Fig. 1 and Tab. 2. Figure 2 represents basic logic XOR gate structure

Fig. 1. XOR gate.

T a b l e 2. Truth table of XOR gate.

A	*B*	*Y*
0	0	0
0	1	1
1	0	1
1	1	0

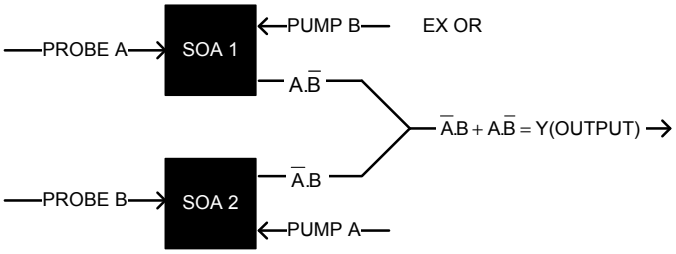

Fig. 2. XOR using SOAs.

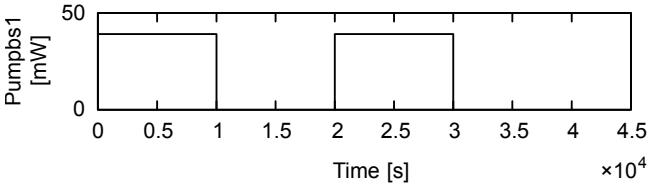

Fig. 3. Input B = [1 0 1 0].

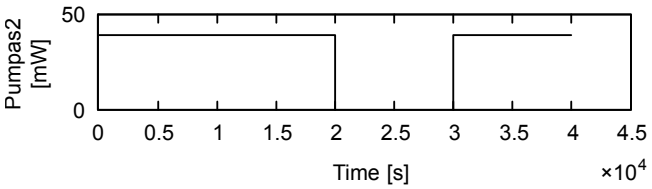

Fig. 4. Input A = [1 1 0 1].

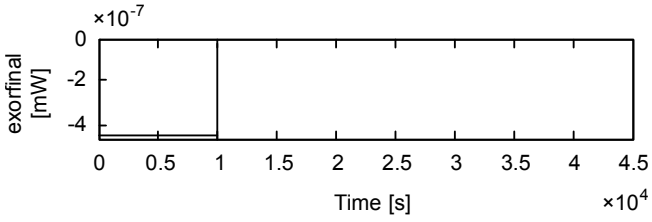

Fig. 5. XOR Output = [0 1 1 1].

using two SOAs. With proper manipulation of pump and probe signal the truth table is verified. The waveform 1 shows an XOR output with input A = [1 1 0 1], and B = [1 0 1 0]. For these pulses of inputs, the generated output is [0 1 1 1]. This verifies the truth table of XOR gate.

The above Figs. 3–5 show that if the inputs (A, B) as (0, 1) or (1, 0) are applied to SOA as shown in Fig. 2, it results in a high output and for the rest combination outputs are logic 0.

Now to implement 4-bit parity generator, we need three XOR gates connected as shown in Fig. 6. The whole circuit is designed with the help of 6 numbers of SOAs. The output is verified with the help of the truth table.

Figure 6 shows that when the three XOR gates are connected properly as shown, the resultant output is a parity generator circuit which can be tested and verified with the help of the truth Tab. 3.

In Figure 7 the outputs of SOA1 and SOA2 are represented as Y. This output acts as an input probe of SOA4 and an input pump of SOA3. Next, the resultant outputs of

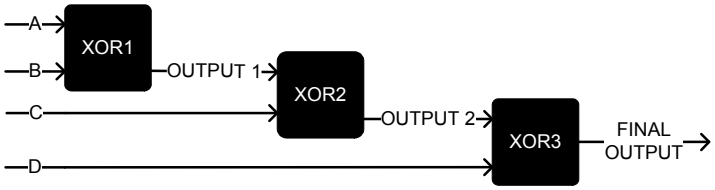

Fig. 6. Parity generator using three XOR gates.

T a b l e 3. Truth table of parity generator.

A	*B*	*C*	*D*	*W*
1	1	1	1	0
0	1	0	0	1
1	0	1	1	1
0	1	0	0	1

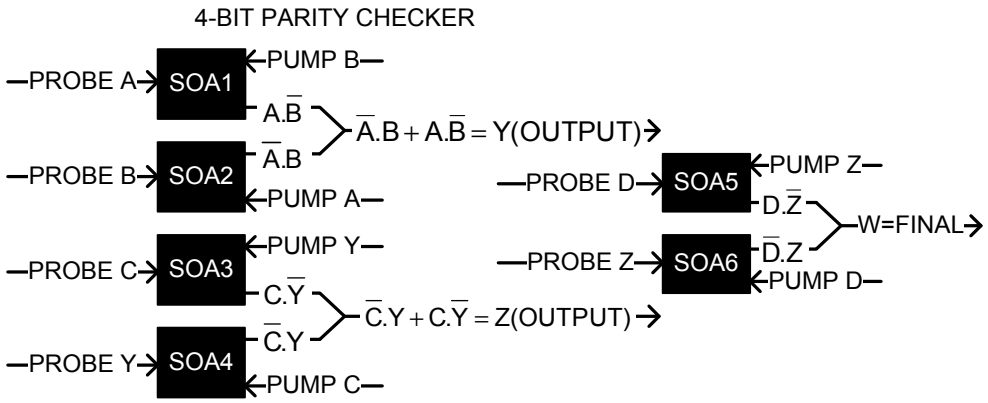

Fig. 7. 4-bit parity generator using six SOAs.

SOA3 and SOA4 are represented as *Z*. This output *Z* acts as an input probe to SOA6 and an input pump to SOA5. The final output *W* represents the function of a parity generator.

Figures 8–12 show that when the inputs $A = [1\ 0\ 1\ 0]$, $B = [1\ 1\ 0\ 1]$, $C = [1\ 0\ 1\ 0]$ and $D = [1\ 0\ 1\ 0]$ are applied, the resultant output is [0 1 1 1],which verifies the fact that an output result is 1 when the number of 1s in an input (*A*, *B*, *C*, *D*) is odd and

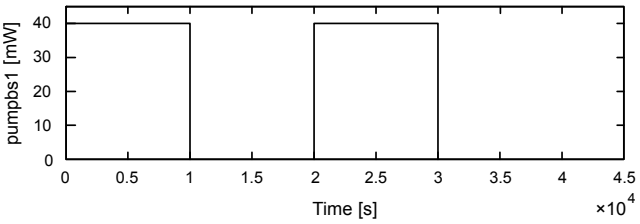

Fig. 8. Input $B = [1\ 0\ 1\ 0]$.

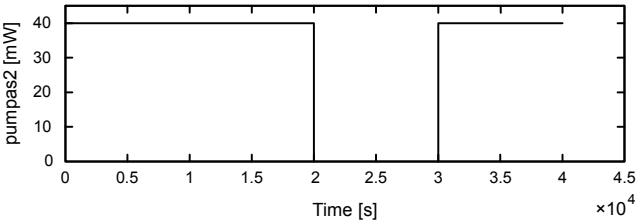

Fig. 9. Input $A = [1\ 1\ 0\ 1]$.

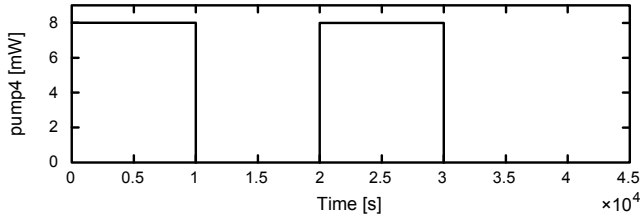

Fig. 10. Input C = [1 0 1 0].

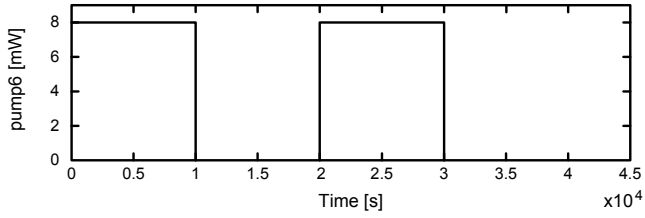

Fig. 11. Input D = [1 0 1 0].

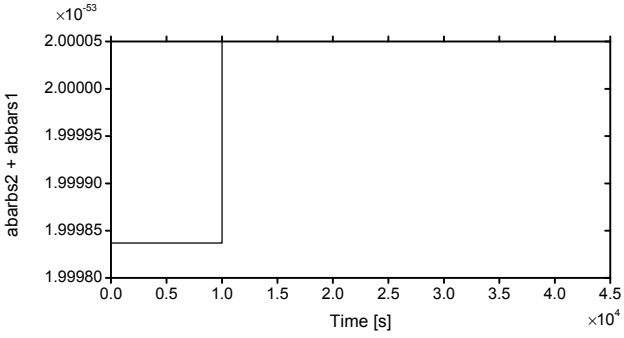

Fig. 12. Output of parity generator = [0 1 1 1].

also an output result is 0 when the number of 1s in an input (A, B, C, D) is even. This is the basic feature of a parity generator.

4. Conclusions

The parity check is one of the most widely used binary manipulations in electronic logic and has a variety of applications in data communications and computing. Typically, a parity bit is attached to a binary word before transmission of the data so that the receiver has the ability to verify the integrity of the recovered digital data. In conclusion, we have successfully demonstrated an all-optical parity checker scaleable in operating speed to the fastest switching speed of the all-optical gates using XGM effect.

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