

Mitigating timing errors in time-interleaved ADCs: a signal conditioning approach

Abhishek Ghosh, *Student Member, IEEE* and Sudhakar Pamarti, *Member, IEEE*
 Department of Electrical Engineering, University of California, Los Angeles, CA 90095
 Email: {abhishek,spamarti}@ee.ucla.edu

Abstract—Novel techniques based on signal-conditioning are presented to mitigate timing errors in time-interleaved ADCs. A theoretical bound on the achievable spurious signal content, on applying the techniques, is also derived. Behavioral simulations corroborating the same are presented.

I. INTRODUCTION

Analog-to-digital converters (ADCs) form the interface between natural systems, which are essentially analog, and the digital regime of processing machines. Ever-escalating data rates have imposed severe challenges on the design of ADCs in terms of bandwidths of the signals that need to be digitized catering to communication circuits. Furthermore, complex modulation schemes invoked for higher spectral efficiency engender signals having very large dynamic ranges [1]. Such signals demand to be digitized with a very high resolution in order to preserve their fidelity. Consequently, modern ADCs need to be of very high resolution (>12 bits) operating at extremely high speeds (in the GHz) to cater to the evolving communication sector.

To that end, several architectures have been proposed which can operate on signals having large bandwidths as well as high dynamic ranges. Time-interleaved architectures have proved to be one of the most suitable candidates for this purpose. Let's take a closer look at a time-interleaved ADC.

A. Time-Interleaved ADCs: modeling

The basic architecture is illustrated in Fig. 1. The incoming signal $x(t)$ is processed by L parallel branches, such that each branch operates on the signal with a time-period LT_S where T_S is the overall sampling time for the ADC, satisfying $F_S = 1/T_S$ (F_S is the sampling frequency). It is assumed that $x(t)$ is a band-limited signal with a bandwidth B such that $F_S > 2B$ (the familiar Nyquist relation). The main advantage of the time-interleaved architecture hence becomes evident. Since each individual branch operates only at a speed F_S/L , hence realization of a single ADC becomes quite feasible and economical at a nominal power expense. The digital outputs of each individual ADC $y_i[n]$ where $i \in [1, L]$ are combined to result in the final digital output $y[n]$.

Time-interleaved architectures, though seemingly very elegant, are plagued with issues attributed to mismatches between the individual branches. Three main mismatch sources can be identified, namely

- DC offsets
- Gain mismatches

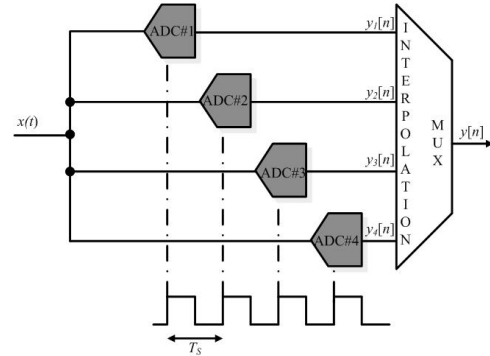


Fig. 1: Time-Interleaved ADC: concept

- Timing mismatches

Out of these three, the first two have been dealt in literature extensively, and satisfactory, low-cost solutions have been identified to mitigate their effects. The main ideas behind these solutions stem from estimating the aforementioned errors and then calibrating the system to counter them. The first two are easy to counter since channel-specific gain control and DC offset control/cancellation are easy to achieve in a power-economical way [2]–[4]. However, calibrating for phase mismatches (timing mismatches) proves to be a much more tedious task [5], [6]. Several techniques have been proposed in literature to alleviate the problem of timing-mismatches.

B. Prior-art

Most of the techniques to tackle timing mismatches are based on calibrating the inter-channel timing error(s) and then *shifting* the sampling edge for each channel based on some form of digital filtering to match the correct edge using any form of digitally controlled delay elements [7]–[11]. Subtle differences can be found though, among these techniques and hence merit some discussion for developing the proposed idea. In [7], a digital detection subsystem (DDSS) and a digitally-controlled delay element (DCDE) operate in a negative feedback loop for each channel to adjust the timing edge based on the digital control word corresponding to each channel mismatch. The precision of the edge-matching obtained in this technique, however is based on the size of the digital-to-time converter step-size t_{step} (which may be poorly controlled over process, voltage, temperature variations) and hence can limit the overall SNR for high performance systems. In [8], a

master clock is used to synchronize all the sub-clocks, that thrusts a great reliance on the accuracy of laying out the channels symmetrically with a robust clock-distribution tree, which may not be feasible for most practical considerations. In [9], an interesting correlation based technique is used to estimate the timing-skews for each channel with respect to a reference channel. The estimation method relies on maximizing the SNR for each channel by moving the timing-edge (similar to gradient algorithms predominant in adaptive filters). The timing-edge is adjusted using a cascaded delay-line, implemented using variable capacitive loading through digital bits from the correlation mechanism. Although this work achieves excellent timing resolution but its dependence on PVT operating conditions makes it infeasible for a robust system. An interesting idea to correct for timing mismatches is proposed in [10], where the ADC outputs are digitally filtered (to implement an all-pass transfer function) to impart phase delays corresponding to Δt_i (phase skew in i -th channel). Practical considerations enforce the filters to be windowed using optimization algorithms. This technique, though somewhat independent of the *minimum timing resolution*, will naturally operate better for very high-order filters rendering a large power consumption operating at the sub-ADC frequency.

In this paper, we propose a digital signal conditioning technique to allay the timing-mismatch errors. The main difference from most of the prior-art lies in the fact that an exact alignment of the sampling edge with the correct edge for a particular channel is *not effected at all times*. However, it is ensured that on an average the sampling edge coincides with the exact edge. Also, the instantaneous errors, so committed are spectrally shaped out-of-band or scrambled depending on the resolution/power tradeoff.

It should be noted that the former (shaping the instantaneous errors) will be beneficial only for narrow signal bands of interest that are spread over a wide spectrum: particular examples of which maybe bandpass delta-sigma ADCs. The shaping technique in particular, consequently, is not applicable to Nyquist ADCs since out-of-band errors are not suppressed, thereby degrading the (signal-to-noise and distortion ratio)SNDR of the system. The proposed approach enables about 30dB of (spurious-free dynamic range)SFDR improvement over the uncorrected case, as detailed in Section III, decoupling the efficacy of the technique with the minimum timing resolution attainable in a particular CMOS technology node.

The paper is organized as follows. Section II presents the proposed technique. Behavioral simulation results are discussed in Section III while the paper is concluded in Section IV.

II. PROPOSED TECHNIQUE

A. Theory

Let the input to the system be $x(t)$. The sampling time for the i -th ADC, with a timing skew of τ_i , is

$$t_i[n] = t_{i,ideal}[n] + \tau_i \quad (1)$$

where $t_{i,ideal}[k]$ is the ideal sampling time at the k -th time instant.

The proposed technique bears analogy with a fractional-N PLL multi-modulus divider [12]. Let Δ be a well-defined circuit quantity ($\Delta \gg \tau_i$). Then it suffices to jump between the edges defined by $\mathcal{E} = t_i[n] \pm k\Delta, \forall k \in \mathbb{N} \cup \{0\}$ in a definite manner to converge on to the exact edge in an average sense.

The proposed idea is illustrated in Fig. 2. With an estimate of the timing errors, τ_i between the branches (through post-calibration), a digital sequence $r_i[n]$ is generated for the i -th channel as shown. The different timing edges $\in \mathcal{E}_1 \subset \mathcal{E}$ are then chosen based on the sequence $r_i[n]$ (due to hardware constraints, a smaller set \mathcal{E}_1 is chosen). The cardinality of the set (and hence the span of $r_i[n]$) \mathcal{E}_1 is determined based on the available hardware complexity and power-cost. Now, the sampling instant can be expressed as,

$$t_i[n] = t_{i,ideal}[n] + \tau_i + r_i[n]\Delta \quad (2)$$

Hence, the sampled signal for the i -th channel can be represented as (in a Taylor's series approximation)

$$x_i[n] = x(t) + (\tau_i + r_i[n]\Delta) \frac{dx(t)}{dt} + \frac{(\tau_i + r_i[n]\Delta)^2}{2} \frac{d^2x(t)}{dt^2} + \dots \Big|_{t=t_{i,ideal}[n]} \quad (3)$$

Hence, it suffices to cancel the error terms $(\tau_i + r_i[n]\Delta) \frac{dx(t)}{dt}, \frac{1}{2}(\tau_i + r_i[n]\Delta)^2 \frac{d^2x(t)}{dt^2}$ by an appropriate selection of the sequence $r_i[n]$. In other words, the signal conditioning techniques would attempt to generate sequences $r_i[n]$ that will ensure the following two conditions:

- (a) $\mathbb{E}(\tau_i + r_i[n]\Delta) = 0$
- (b) $\mathbb{E}((\tau_i + r_i[n]\Delta)^2)$ is bounded

Based on this theory, we propose the scrambling technique.

B. Scrambling the timing errors

We choose the edge set $\mathcal{E}_1 = t_i[n] - \Delta, t_i[n], t_i[n] + \Delta$. We propose to select each one of these edges corresponding to the set $r_i[n] = \{-1, 0, 1\}$ with an element-wise correspondence. Let us assign the occurrence probabilities of the values of $r_i[n]$ as p_{-1}, p_0, p_1 where the notations are self-explanatory. Then, we can construct,

$$\begin{bmatrix} 1 & 1 & 1 \\ (1 - \alpha_i) & -\alpha_i & -(1 + \alpha_i) \\ (1 - \alpha_i)^2 & \alpha_i^2 & (1 + \alpha_i)^2 \end{bmatrix} \begin{bmatrix} p_{-1} \\ p_0 \\ p_1 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ g^2 \end{bmatrix} \quad (4)$$

where g is a small constant independent of all the ADCs and $\alpha_i = \tau_i/\Delta$ subject to the condition $\{p_{-1}, p_0, p_1\} \in [0, 1]$.

The three equations in Eqn. 4 can be understood intuitively:

- $\{-1, 0, 1\}$ is the span of $r_i[n]$
- The timing errors go to zero on an average
- The second-order error term is a constant independent of the ADCs

Remark: The last statement should be noted carefully. The error introduced due to the second term is independent of the

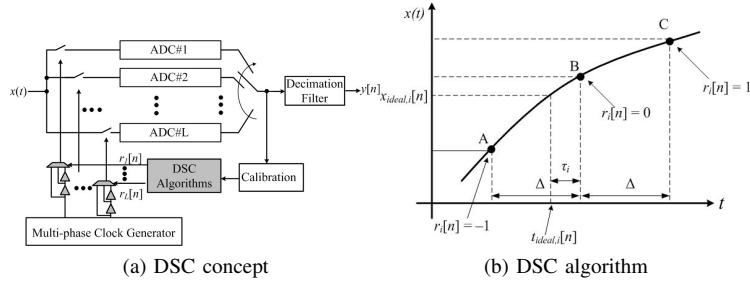


Fig. 2: Digital Signal Conditioning

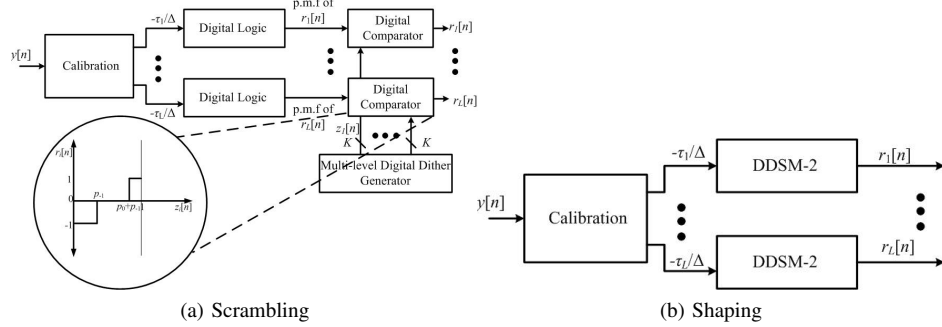


Fig. 3: DSC techniques

individual ADCs and loses potency to cause spurious tones (for a tonal input). The error power is instead spread over the entire band (scrambling) [13]. Depending on the value of g and the oversampling ratio in the ADCs, the resultant SNR hit needs to be evaluated. The higher-order terms may still engender some residual non-linearity, but they are negligible for all practical purposes.

Implementation of the digital signal conditioning (DSC) block in Fig. 2 is shown in Fig. 3(a). Eqn. 4 is solved to determine $\{p_{-1}, p_0, p_1\}$. Subsequently, a K -bit digital dither ($\in [0, 1]$) is passed through a quantizer with its thresholds set by $\{p_{-1}, p_{-1} + p_0, 1\}$ to generate the sequence $r_i[n]$. The technique is able to cut down the spurious tones by almost 20dB as illustrated in the next section.

C. Spectrally shaping the timing errors

The main idea proposed in this section is to generate the sequence $r_i[n]$ using a digital delta-sigma modulator (DDSM) as explained below. We assume having the estimate of the timing mismatch error τ_i in K bits such that the selected edge converges in mean to the correct edge. The instantaneous error, so introduced, is now spectrally shaped out-of-band. A subtle but important point should be noted here. Even though the residual timing error is shaped out-of-band, since this error is different across channels, some residual second-order non-linearity may show up as spurious tones, but it can be proved theoretically (and substantiated through simulations), this error contribution is typically much lower than the accepted quantization-error of the ADC, and hence does not cause an issue. The technique is illustrated in Fig. 3(b). The negative of

the timing-error for each channel, $-\tau_i$, scaled by the quantity Δ , is passed through a digital delta-sigma modulator (DDSM) of order P with M output levels and the output of this DDSM is the control sequence $r_i[n]$. It should, however, be kept in mind that a DDSM is prone to producing idle tones unless certain conditions are satisfied [14]. It has been proved in literature [14], that the input to the DDSM should be bounded in $[-(M+1-2^P)\frac{a}{2}, (M+1-2^P)\frac{a}{2}]$, where a is the step-size of the quantizer to prevent its overload. To further reduce the effect of limit-cycle tones, a small random signal $d[n]$ having the statistics $\Pr(d[n] = 0) = \Pr(d[n] = 1) = 0.5$ is added to the K bit input (LSB dithering) [16]. The output sequence $r_i[n]$ has an average of $\frac{-\tau_i}{\Delta}$ while its quantization error power is spectrally second-order shaped out of band [15]. The second-order error term for the i -th channel from Eqn. (3) is the dominant residual error (since the first-order term is driven to zero by the design of the DDSM). The analysis becomes intuitive for a tonal input. Let $x(t) = A \sin(\omega_0 t)$. Then, evaluating the RHS of Eqn. 3 and extending to the cumulative error, we find,

$$\begin{aligned}
 e[n] &= - \sum_{i=1}^{i=L} \frac{1}{2} \mathbb{E}(\tau_i^2 + r_i[n]^2 \Delta^2 + 2\tau_i r_i[n] \Delta) \\
 &= - \sum_{i=1}^{i=L} \frac{1}{2} \mathbb{E}(-\tau_i^2 + r_i[n]^2 \Delta^2) A \omega_0^2 \sin(\omega_0 t) |_{t=t_{i,ideal}[n]} \\
 &= \sum_{i=1}^{i=L} \frac{1}{2} (\tau_i^2 - S_i \Delta^2) A \omega_0^2 \sin(\omega_0 t) |_{t=t_{i,ideal}[n]} \quad (5)
 \end{aligned}$$

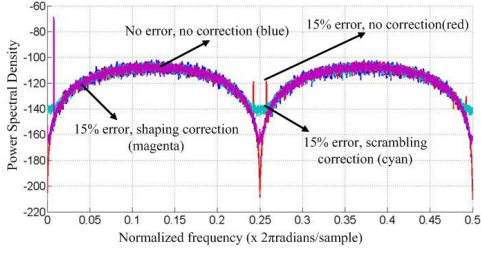


Fig. 4: Output spectrum: different scenarios

where $S_i \triangleq \mathbb{E}(r_i[n]^2)$. In this analysis, it is assumed that the channels are time-offset from a reference channel by the error τ_i . Treating any one channel (k -th one) as the reference channel makes $\tau'_k = 0$ where $\tau'_i = \tau_i - \tau_k$. This observation does not distract from the given analysis and can be easily accounted for.

Now, it should be seen from [16], that in a properly designed DDSM, since the error samples are independent of the input samples, hence for a P -th order DDSM, the output variance of any $r_i[n]$ can be written as,

$$\mathbb{E}(r_i[n]^2) = \frac{a^2}{12} f(P) + \frac{\tau_i^2}{\Delta^2} \quad (6)$$

where a is the step-size of the quantizer in the DDSM, $f(\cdot)$ is a bounded function of the loop-filter order.

This error variance, is thus bounded for any given P as long as the no-overload condition for the DDSM quantizer is satisfied. In fact, the resultant SFDR of the ADC can be written as

$$\text{SFDR} = 10 \log_{10} \left(\frac{4}{\omega_0^4 \sum_{i=1}^{i=L} (S_i \Delta^2 - \tau_i^2)^2} \right) \quad (7)$$

III. SIMULATION RESULTS

The simulation test-bench is described now. The input $x(t)$ is chosen to be a sinusoid. L , number of channels is chosen to be 4. Each channel ADC is configured to be a second-order sigma-delta ADC with 8 output levels. The shaping technique is shown for a second-order DDSM with four output levels i.e. $r_i[n] \in \{-3, -1, 1, 3\}$, which implies $a = 2$ in Eqn. (6). For a 4-way interleaving, the noise-shaping nulls (from the actual ADC as well as from the DDSM) form at $F_S/4$. Timing-errors show up as spurious tones around the null at $F_S/4$. The ADC output spectrum is illustrated for the ideal scenario with no errors, for the timing errors with no correction as well as for both the techniques (scrambling and shaping) in Fig. 4. As can be seen, the scrambling technique eliminates almost all channel-dependent errors resulting in an elevated noise-floor mainly corresponding to the g term from Eqn. 4. For the shaping case, the spectral nulls are much deeper as expected, the residual noise being attributed to the residual error terms in Eqn. 6. In fact, for a 2nd-order DDSM with four output levels, it can be shown that the SFDR due to 15% timing error is about 90 dB, which should satisfy almost all practical communication scenarios. For the uncorrected case,

the timing error begets spurious tones around the null at $\pi/2$, degrading the SFDR to about 60 dB.

IV. CONCLUSION

Digital signal conditioning based techniques for mitigating timing mismatch errors in time-interleaved ADCs are proposed. Two power-efficient techniques, one based on scrambling the error components and another based on spectrally shaping the error components have been presented, their operations analyzed and their performances substantiated through behavioral simulations.

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