A Novel Optoelectronic Device Complimentary to Photodetector

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Abstract: We experimentally demonstrate the first complimentary device to photodetector – output current decreases upon shining light. The device enables receiver-less optical interconnect scheme in conjunction with a conventional photo transistor.
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1. Introduction

Interconnect is expected to be a major problem in future high performance silicon chips in terms of latency, power and bandwidth. Optical on-chip interconnect has potential benefits to solve these problems. Because of very high carrier frequency, optical interconnect avoids the metal waveguide and resistive loss physics, thus high bandwidth is achievable. However, for short interconnect, energy/bit is still high compared to conventional copper wire. Some optical modulators [1] and lasers [2] approach power requirement for on-chip optical interconnect, but photodetector and receiver circuit still consume high power. While photodetector should not pose a basic challenge in power requirement, receiver circuit consume high power, and it only slowly decreases as technology node shrinks [3]. Receiver circuit is expensive in terms of both footprint and power dissipation.

To decrease receiver-end power consumption, receiver-less scheme has been proposed. To realize this, as shown in Fig. 1, we need a device which can operate as complimentary to the photodetector, i.e. decrease output current upon shining light, so can be used in conjunction with conventional photo transistor [4]. Utilizing band bending and gate depletion, we have demonstrated the first complimentary device to photodetector.

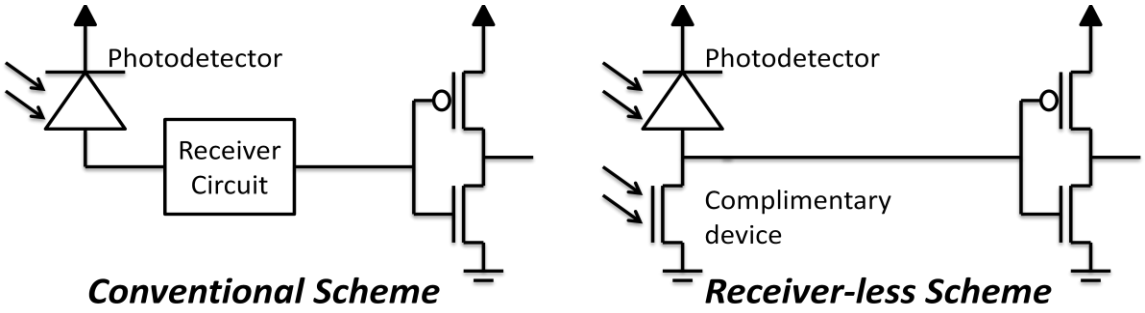

Fig. 1. Conceptual circuit diagrams for conventional optical receiver scheme and receiver-less scheme.

2. Operation mechanism

Fig. 2 shows device structure, an upside down MOSFET. With relatively low doping concentration (~$10^{17}$$cm^{-3}$) in the bottom p-type Si gate and high doping concentration (~$10^{20}$$cm^{-3}$) in the ultrathin (5nm or 7nm) polysilicon channel, the gate is initially depleted. Fig. 3 shows band diagram in vertical slice and Fig. 4 shows in horizontal slice.

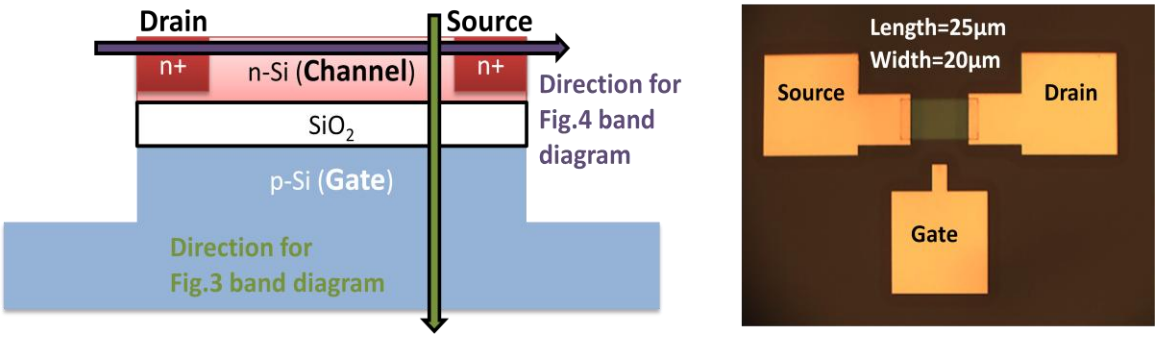

Fig. 2. Device side-view diagram and top-view photo image.

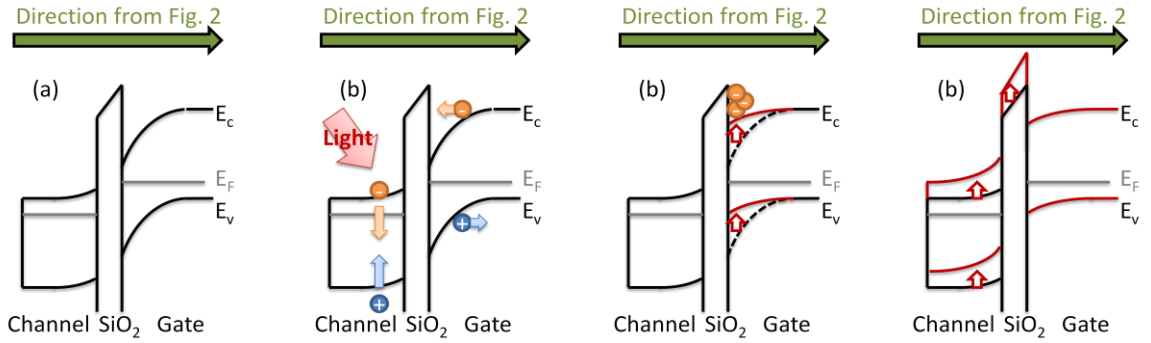

Fig. 3. Band diagrams of vertical slice of the device under incident light.

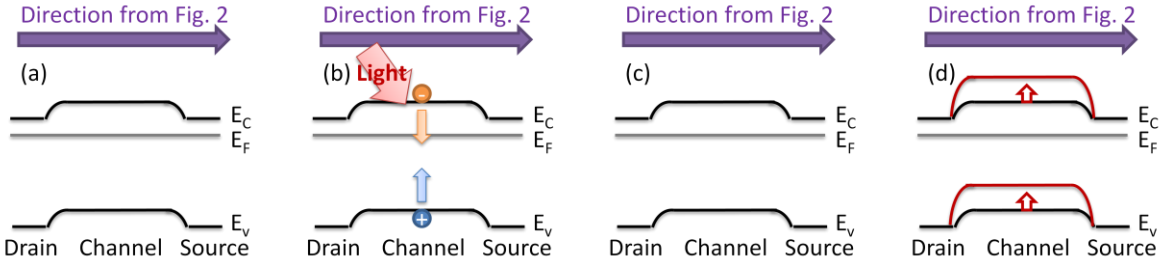

Fig. 4. Band diagrams of horizontal slice of the device under incident light.

Operation mechanism is as follow. (a) Since channel is n-type polysilicon and source/drain are heavily doped n-type, current normally flows from source to drain. (b) If light is incident onto the device, electron-hole pairs are generated in both depletion region of the Si gate and polysilicon channel. These electron-hole pairs generated in depletion region in gate are separated because of band bending in the gate. However, since channel is polycrystalline and highly doped, electron-hole pairs generated in channel quickly recombine, and negligible photocurrent is generated. (c) While holes are swept to bottom of the gate electrode, electrons pile up at gate-oxide interface. The electron pile-up pulls up band at gate-oxide interface and relaxes band bending in the gate. (d) To compensate the band bending relaxation, band bending occurs in the channel instead, which increases barrier between source and drain.

Careful design in thickness and doping concentration of the channel enables full depletion upon light shining and effectively cut-off or reduce drain current. The device operation can also be viewed as modulation of voltage by light shining at gate-oxide which controls output current in the depletion mode MOSFET.

3. Fabrication

We used p-type Si doped to $10^{17}cm^{-3}$ as starting substrate. Then 10nm of thermal oxide is grown to be used as gate dielectric. On top of the gate dielectric, 5nm to 7nm thick n-type polysilicon in-situ doped to $10^{20}cm^{-3}$ is deposited by LPCVD and subsequently annealed at 900C for 3 hours. 10nm of low temperature SiO_2 (LTO) is deposited on top of the channel for protection. Then polysilicon channel and 100nm of substrate are dry etched to isolate the device. LTO is again deposited to protect polysilicon sidewalls. Then LTO is etched to create contact holes. The device is doped in PH_3 environment at 800C for 20min to create low resistance S/D contacts followed by Ti metallization. The process is explicitly CMOS compatible. As a first pass, we measured 20x25μm device.

3. Result

For the optical measurement, we used 850nm wavelength laser as light source focused on 6nm diameter. Left graph of fig. 5 shows basic operation observed for the device with channel thickness of 5nm and drain voltage of 1V. With incident light, I_d is decreased. Target operation should be around threshold voltage, where output current should be high without incident light but still have good turn on/off ratio. One thing to note is that, I_d-V_g curves have constant horizontal spacing, due to the mechanism that device is modulated by voltage modulation at gate-oxide interface, not by photocurrent directly. Right graph of fig. 5 shows voltage shift for different incident light power. Since the voltage modulation originates from relaxing band bending in the gate, it is obvious that there should be maximum voltage shift. In this device, maximum voltage shift of 0.57V is demonstrated, which is enough to be used in receiver-less scheme (Fig. 1). The figure also shows that in relatively low light, voltage shift is linearly dependent on logarithm of incident power. This also corresponds to operation mechanism and is expected through simulation.

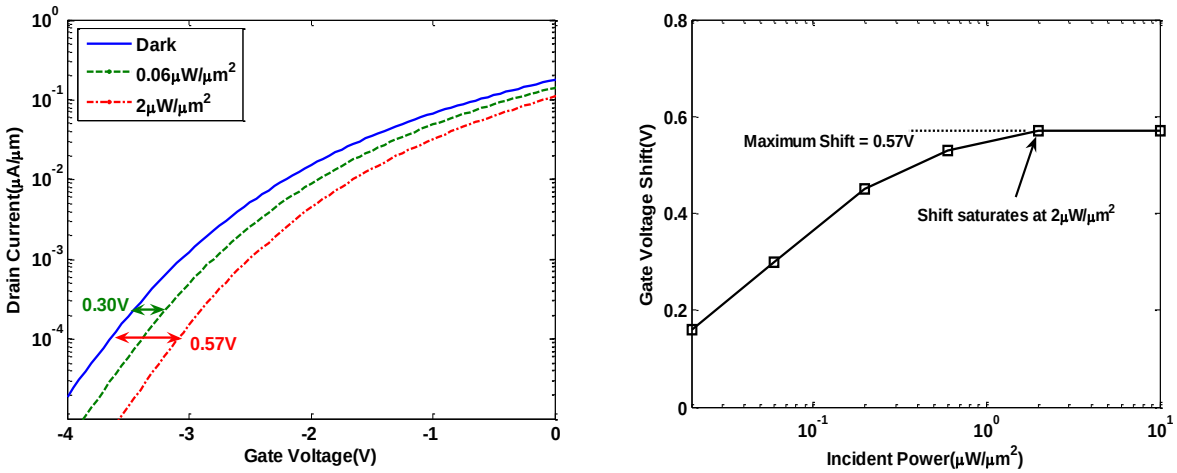

Fig. 5 I_d-V_g and gate voltage shift of the device with 5nm-thick channel

Though device with 5nm-thick channel is more suitable for proof of concept, device with 7nm-thick channel shows better characteristic. 7nm channel is chosen because it is in between maximum depletion width of the channel under dark and under intense light. Fig. 6 shows I_d-V_g curves under different light intensity, again with drain voltage of 1V. Without light, channel is not cut-off because it is thicker than maximum depletion width. Increasing incident light intensity increases maximum depletion width, and around 0.3μW or 0.6nW/μm^2, channel finally starts to cut-off. With this design, we demonstrated very high on/off contrast (0.11μA/μm or 2.2μA to 0.0016μA/μm or 0.032μA at -3V) under only 0.6nW/μm^2 of incident light.

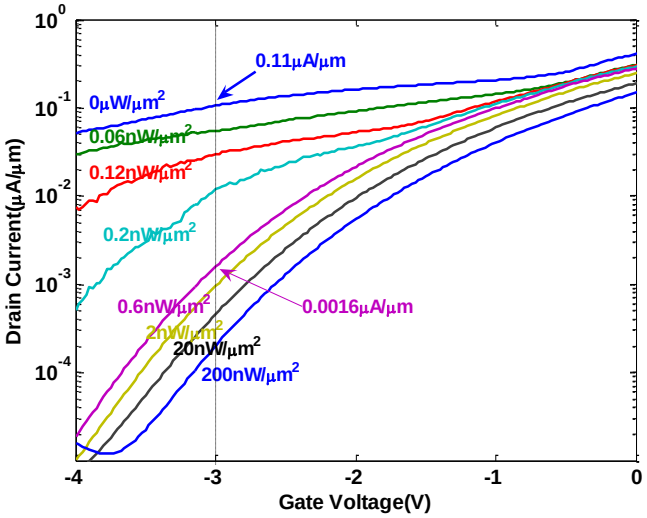

Fig. 6 I_d-V_g and gate voltage shift of the device with 7nm-thick channel

4. Conclusion

We have experimentally shown the first complimentary device to photodetector with output current reduction with light incident. The device is explicitly CMOS compatible and highly scalable. We have successfully observed voltage shift of Id-Vg curve as big as 0.30V in 0.06μW/ μm^2 and maximum voltage shift of 0.57V in 2μW/μm^2 in 20x25μm device. We also observed that with careful design, 0.11μA/μm of current can be cut-off to 0.0016μA/μm under only 0.6nW/μm^2 of incident light.

4. References

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