Novel ODU path switching for ODU reallocation without bit disruption using dynamic delay control scheme

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Abstract: A novel ODU path switching using dynamic delay difference compensation for ODU reallocation without bit disruption is proposed. The proposed bit-loss-free path switching is successfully demonstrated for 10Gbit/s ODU2 path.
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1. Introduction

IP traffic keeps on increasing and the traffic characteristics are changing dynamically due to the diversification of network services. IP packets are mainly transported using Ethernet interface in LAN environments. Furthermore, demands is growing for the wide area transport of packets. Enhanced OTN (Optical Transport Network) can accommodate these demands.

In the near future, frequent setup and tear-down of various size ODU (Optical Channel Data Unit) paths will be necessary, then it will cause unused timeslots far from optimized usage of the wavelength resources. An optimization of the whole network is very important for the purpose of cost reduction. In-service reallocation of ODU path could be one solution for the optimization [1, 2]. However, it is easily anticipated that an instantaneous data loss during the reallocation would be an issue, since the loss is solely caused by carrier's motivation.

When the bit rate of a transported signal rises, the volume of data lost due to dynamic path switching rises for the same signal loss time. Therefore, a hitless switching method with no bit disruption is important to provide service with high reliability and quality. So far, hitless switching for SDH electrical paths has been proposed, but the technique supports only fixed and pre-assigned paths [3].

This paper proposes a novel ODU path switching scheme with dynamic delay difference compensation for ODU reallocation without bit disruption. This scheme can dynamically adjust the delay difference between the working and protection path by simple read clock (CLK) frequency control of the stored FIFO (First-in first-out) memory. A concept-level experiment on an OTU2 signal is successfully demonstrated.

2. Principle of ODU path switching without bit disruption using dynamic delay control

A schematic diagram of ODU path switching without bit disruption based on dynamic delay control is shown in Figure 1. In the transmitter, data is duplicated with one copy sent by the working and the other by the protection path. In the receiver, each signal is received by ODU CDR (Clock and Data Recovery) and recovered ODU data is temporarily stored in FIFO memory. The value of MFAS (Multiframe Alignment Signal) of each signal is detected in the OH monitor and input into the delay difference detector. This detector checks the relative delay difference between MFAS values of working and protection paths. The information indicating the control amount is given to a clock controller on the side whose delay should be adjusted. The clock controller controls the delay by adjusting the amount of data stored in memory. After the delay difference is compensated, ODU path switching operation enters its standby phase, and the path is switched from the working to protection with no bit disruption as directed by the operator. Figure 2 shows the details of dynamic delay difference compensation. To control the delay, the clock controller uses the clock, synchronized to the ODU signal, as FIFO memory writing clock; its frequency is slightly desynchronized as a reading clock. In the case of (a) increasing the delay, the frequency of the reading clock is lowered from that of the synchronous clock for a certain period and then returned to the synchronous state. The delay is increased because the amount of stored data in FIFO memory is increased by the frequency difference between writing and reading clocks. On the other hand, in the case of (b) decreasing delay, the frequency of the reading clock is raised from that of the synchronous clock for a certain period and then returned to the synchronous state. The delay is decreased because the amount of stored data is decreased. The frequency shift and period are set by the delay control information.

Delay of the working path is controlled in the following cases while service is continued.

Case 1: the protection path is longer than the working path, and delay of the latter should be increased.

Case 2: protection path is shorter than the working path, but the memory consumed by the working path is so large that it is more convenient to reduce the delay of the working path.

When the proposed scheme adjusts the delay of the working path, care is needed because of the resulting change in the client's frequency.

1. Frequency (Bit rate) tolerance of client service and equipment
   Clock accuracy requirements of OTN, SDH, and 10Gbit/s Ethernet are +/-20 ppm, +/-4.6 ppm, +/-100 ppm, respectively. It's necessary to control the clock frequency so that these limitations are not exceeded.
2. Bit slip tolerance of client service and equipment
   Some of the client's devices use phase-locking to a network synchronization clock. When a frequency shift continues for some time, a bit slip can occur in such devices. The bit slip tolerance depends on the memory capacity of the device. Devices that are synchronized to the rate of the transmitted signal (e.g. Ethernet), have no such problems. (Applicability to Sync Ethernet is for further study.)

3. Experiments

The proposed ODU path switching scheme was implemented on an FPGA and subjected to concept level testing. The experimental setup to evaluate no bit disruption ODU switching is shown in Fig. 3. For convenience, OTU2 signal is used as input and output signal for ODU2 path. OTU2 from an OTN analyzer was divided in two by optical coupler, and each signal (working and protection) was transmitted via different fibers to the evaluation board. The operation of the evaluation board was controlled by PC-sourced commands such as setting the amount of frequency shift, starting dynamic delay control, and selector switching. Information of current delay difference, FIFO occupancy, was monitored by the PC. The OTU2 output by the board was sent to the OTN analyzer, and error and alarm occurrence was observed via the OH and payload monitor function. 1/64 de-multiplexed signals at the point of selector input can be monitored to observe the delay controlled signal (working and protection). The frequency shift of FIFO read clock was observed via a frequency counter. Waveforms of working and protection path (a) before and (b) after delay adjustment are shown in Fig.4. The bit sequences aren't matched before delay adjusting, but the delay difference is offset perfectly by the dynamic delay control scheme. No bit error was detected by the OTN analyzer even during delay adjustment. After the delay difference is eliminated, ODU2 path switching between working and protection path replacing alternately is successfully executed at any number of times. Moreover, we conducted no bit disruption switching for the fault of the transmission fiber cut. We observed bit error free protection switching.

4. Discussion

Figure 5 shows the relation between the delay difference and delay difference adjustment time when the frequency was shifted. It is effective to increase the amount of frequency shift to shorten the delay adjustment period, but this raises the risk of exceeding the bit rate tolerance limit. For example, a frequency shift of 0.1 ppm is enough to correct the delay difference of 1,000 m under the condition that the adjustment period is limited to less than 100 seconds. If the delay difference is 10,000 m, the frequency shift should be 1ppm under the same time limit. A frequency shift of 0.01 ppm has an insignificant chance of exceeding the bit rate tolerance limit, but the adjustment time is long. It is necessary that operator should know how much frequency shift the device connected to the client side permits before actuate the dynamic delay control. After that, the dynamic delay difference is actuated while a relation with the delay adjustment time and the length of delay difference is considered.

5. Conclusion

We proposed a dynamic delay control scheme to permit ODU path switching for ODU reallocation without bit disruption. A concept-level experiment was successfully demonstrated. The proposed switching scheme is simple to implement and applicable to an optional path, so it is possible to optimize the network while keeping the service quality.

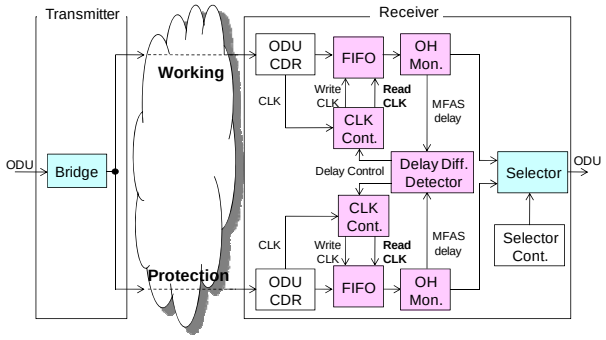

Fig. 1 Schematic diagram of hitless ODU path switching by dynamic delay control technique

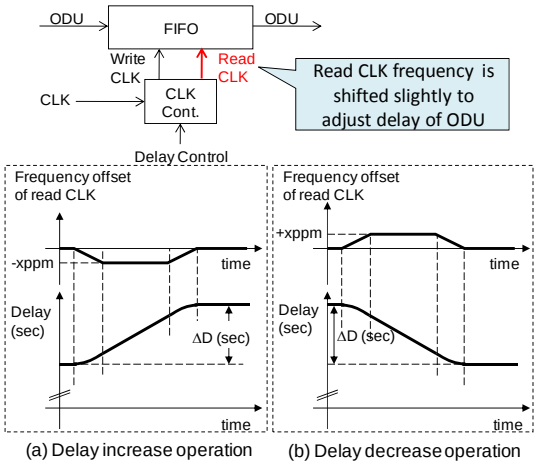

Fig. 2 Dynamic delay control operation by frequency adjustment

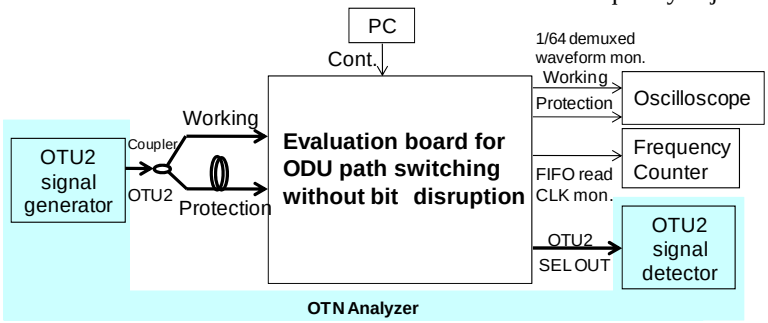

Fig. 3 Experimental setup

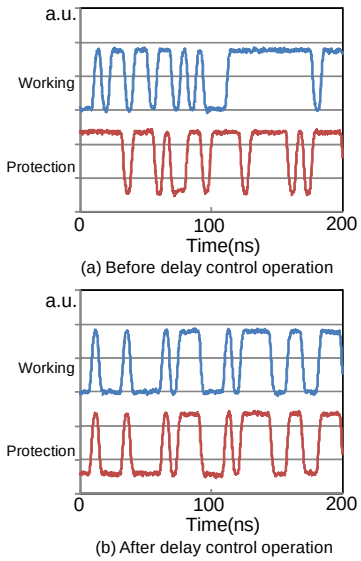

Fig. 4 1/64 de-multiplexed waveforms of working and protection signal at selector input

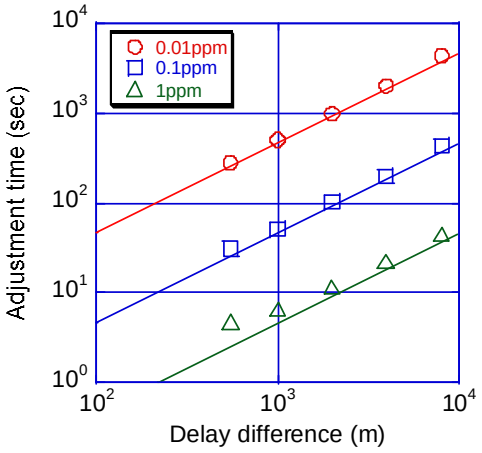

Fig. 5 Delay difference and delay difference adjustment time

4. References

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[3] S. Matsuoka et al.,"Classified Path Restoration Scheme with Hitless Protection Switching for Large-Capacity Trunk Transmission Networks," IEEE GLOBECOM 95, pp.941-945, 1995