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Optical Dynamic Random Access Memory (ODRAM)

Gianluca Berrettini[1], Luca Potì[2] and Antonella Bogoni[2]
1: Scuola Superiore Sant'Anna, via G. Moruzzi 1 56124 Pisa , Italy
2: National Laboratory on Photonic Networks - CNIT, via G. Moruzzi 1 56124 Pisa, Italy
e-mail: gianluca.berrettini@sssup.it

Abstract: An n-bit all-optical dynamic random access memory for write, read and refresh operation in optical computing applications is investigated. The 1-bit memory element obtained by a SOA-based variable optical buffer is verified and characterized.
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1. Introduction

The rising interest of fast and efficient sub-systems for optical computing is leading the research towards the investigation of photonic digital processing. Despite optical devices for digital functionalities are in their early stage and the realization of whole all-optical computing system is still remote, it is proven that photonic processing has the potentiality to overcome electronics due to their high-speed capability. Photonic digital functionalities have been largely demonstrated but the lack of a reliable all-optical memory continues to limit the functional capacity of photonic circuitry. Several schemes for optical random access memory (ORAM) have been investigated [1] [2] especially for optical packet switching networks and commonly addressed as optical packet buffers. These solutions are restricted to synchronous operations, which limits the architecture design and increase the circuitry complexity at time. In a previous work [3] we demonstrated a semiconductor optical amplifier (SOA)-based buffering solution for 10Gbit/s packets which introduced variable buffering time for relatively large delays by means of a more compact footprint with respect to other schemes. Starting by this solution a single bit buffering with true random and asynchronous access can be realized. A static ORAM scheme for asynchronous and variable-length data processing has been demonstrated in [4]. In that solution the use of internal flip-flops and external laser sources to power them provided different output data wavelengths, besides to considerably affect the costs and dimensions of the scheme.

In this paper, a new scheme for a multi-cell optical dynamic random access memory (ODRAM) aiming to reproduce the most analogy with the respective electrical device is proposed. The solution allows for writing and reading operations, as well as refreshing functionality, in an all-optical and dynamic way without any synchronization. The n-bit ODRAM is composed by independent 1-bit memory elements, each one composed by a wavelength preserving SOA-based variable optical buffer proposed in [3]. The cell enabling command, as well as the read and write control signals, are carried out by already demonstrated logic operations between the optical row and column enabling signals. True dynamic random access properties are evaluated for the single cell in terms of extinction ratio (ER) as a function of storage time. 1.77μs bit delay is demonstrated without signal degradation. Multi-cell performance is also investigated. A 3dB ER reduction for an 8x8 matrix structure is measured. The proposed scheme can work as a multi register matrix for synchronous operation, once an n-bit packet is stored in each specific optical buffer.

2. 1-bit memory cell

In a standard electrical DRAM each bit of data is stored in a separate capacitor within an integrated circuit. Since real capacitors leak charge, the information fades unless the capacitor charge is periodically refreshed. In an analogous way, the experimental setup for an all-optical 1-bit memory cell is reported in Fig. 1 (a). It consists of an optical buffer based on a re-circulating fiber loop in which the bit storage time is directly controlled in the optical domain. Two SOAs are used as optical gates enabled alternatively in order to store the packet into the loop or send it to the output. In particular, an optical signal (R) and its logically inverted copy (W) are used as reading and writing control signals to change the gain saturation of SOA_1 and SOA_2, respectively, by cross gain modulation (XGM) non-linear effect. This way, the switching functionality is achieved and the packet can be read or stored by depending on the R and W control signals status. More in detail, during the writing operation a bit is sent into the fiber loop through the optical circulator (OC_1) and the 50/50 optical coupler. In this condition the write signal W is low while the read signal R is high. Therefore, incoming bit finds SOA_1 saturated, whereas it is amplified by SOA_2 and stored for a certain number of rounds into the re-circulating loop. As soon as R and W change their states, the stored bit directly reaches the cell output for reading operation, amplified by SOA_1. At the same time, the SOA_2 is saturated by W and the packet into the loop is suppressed. The last condition acts as loop erasing prior to a new bit storing or a refreshing operation. The specific input bit is sent into the buffer delayed by an optical delay line (ODL) after a bit time (T_b) with respect to the W signal in order reach the loop after that the erasing condition takes place.
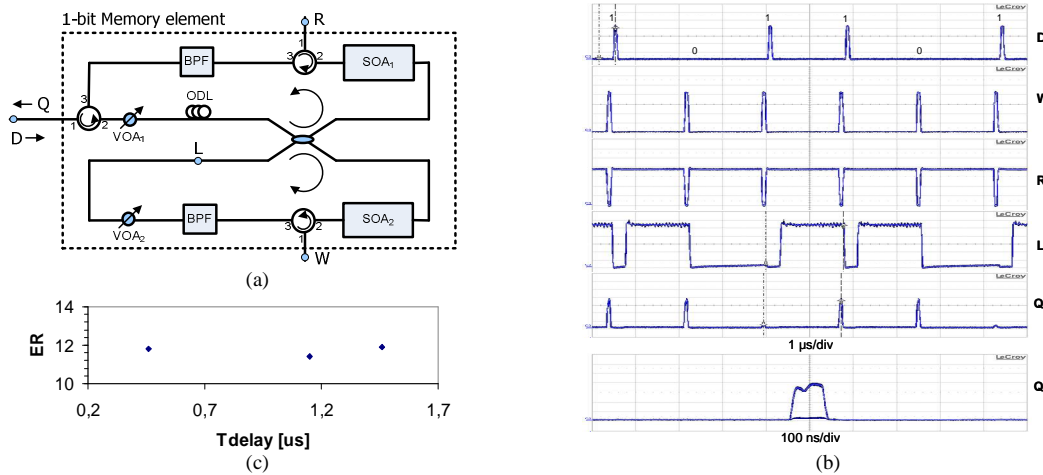
Figure 1. 1-bit memory cell experimental setup based on a variable optical buffer (a). Oscilloscope traces of the signals in each part of the scheme (b). 1-bit memory element output signal ER as a function of the reading delay (c).

The use of an SOA as active element into the fiber loop allows overcoming the power leakage issue during the storage process. The maximum storage time, which is proportional to the maximum number of rounds, is limited by the loop losses and the amplified spontaneous emission (ASE) noise accumulation generated by the optical amplifier. As its analogy in electronics, after a considerable time the memory needs a refresh operation. In this case, the bit circulating in the loop must be erased by saturating the SOA_2 gain and written again. However, by an accurate balancing of the SOA gain and the loop losses, no significant signal degradation can be achieved up to tens circulations without refreshing.

In the specific implementation, the input signal is a continuous wave (CW) at λ_B=1551nm directly modulated by a specific periodic stream of bits [1 0 1] chosen properly to assures the covering of all possible cases, which are the storing and reading of 1, the storing and reading of 0 and the refreshing of 1 after its degrading. The mean power is set to -32dBm by the variable optical coupler (VOA_1). The bit time is T_b=84.6ns and it must be equal to the loop time (T_L) in order to put the bit exactly in line to itself after each round. A bit rate of 562.58KHz is chosen to allows reaching of 20 consecutive bit rounds without refreshing operations for a maximum storage time (T_{delay}) of 1.77μs. The R and W control signals are generated by two CW lasers at λ_R=1547nm and λ_W=1543nm, directly modulated by 562.58KHz electrical square waveforms with a duty cycle of 95% and 5%, respectively, and sent into the SOA_1 and SOA_2 by means of OC_R and OC_W. The R and W signal mean power is set to 6.5dBm and 6dBm. The SOA bias current is set to 200mA (at 27°C), while a variable optical attenuator (VOA_2) allows for setting a proper attenuation to avoid cavity lasing. Two 0.6nm-bandwidth optical band-pass filters (BPFs) in the scheme are needed in order to suppress the out band ASE. The signals at different point of the setup are shown in Fig. 1 (b). Oscilloscope traces report the input bit stream (trace D), the write and read control signals (traces W and R) at the SOA_2 and SOA_1 input, respectively, the signal stored in the fiber loop (trace L), as well as the output bit stream and eye diagram (traces Q) after a storage time of 1.77μs. When a bit 0 is stored in the fiber loop the ASE noise outputs from SOA_2 increase each circulation. For this reason, a weak peak is output when the bit 0 is read. The true random access functionality is demonstrated. The ER of read bits is evaluated as a function of the storage time. Results reported in Fig. 1 (c) shown ER values of 11.9dB, 11.4dB and 11.9dB for T_{delay} of 0.46μs, 1.15μs and 1.46μs, respectively.

3. n-bit Optical DRAM

In Fig. 2 (a) an extension of the previously introduced solution towards an n-bit optical DRAM is proposed. As its equivalent in electronics, ODRAM is arranged in a square array of single cells. For the sake of compactness, a 4-bit ODRAM design is reported, comprising four 1-bit memory cells in a 2x2 matrix structure. Each specific cell is identified by a binary code via row enable (E_R) and column enable (E_C) optical commands. The single cell enabling command (E), the read (R) and write (W) control signal are carried out by well know optical logic function between E_R and E_C signals. In particular, when both E_R and E_C are high, E and R are low as result of a NAND logic gate between E_R and E_C, while W is high as result of NOT E. In this condition the identified cells are enabled for read or write operation. In the write function the writing enable signal (WE) is low and the Gate D is ON. The input bits are forwarded to each 1-bit memory element by means of row and column optical couplers, but only the selected cell is enable to store the data.

E_C	E_R	E	R	W	RE	WE	operation
0	0	1	1	0	-	-	-
0	1	1	1	0	-	-	-
1	0	1	1	0	-	-	-
1	1	0	0	1	0	1	Bit reading
1	1	0	0	1	1	0	Bit writing

(b)

(a)   (c)
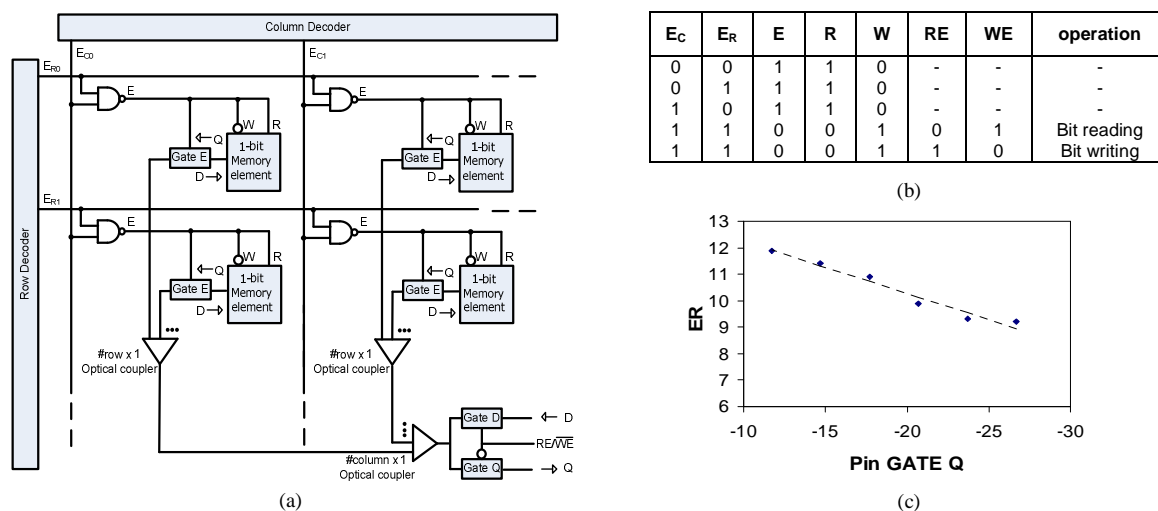
Figure 2. Proposed scheme for a n-bit optical DRAM. In detail a 2x2 matrix structure (a), the truth table reporting the enabling signals, the cell Write and Read commands and the permitted operation (b), and the output signal ER as a function of the gate Q input power (c) are reported.

In the read operation the read enable signal (RE) is low, the Gate Q is ON and the bit coming from the selected cell is extracted. All the gates in the scheme, acting as logical ON/OFF switch, can be implemented by SOAs. In particular, when the enabling signals (E, RE and WE) are high the SOAs gain is saturated by XGM and the gates are OFF. A truth table of the ODRAM is reported in Fig. 2 (b). As the ODRAM capacity grows, the number of the row and column couplers ports scales with the matrix dimension. Because the performances of each single cell are independent and fixed by the loop parameters, the scalability effectiveness of the scheme only depends by the gates input power. Performances are evaluated in terms of the gates output ER as a function of the gates input power. For the sake of simplicity, results for the Gate Q have been reported, which it was noted to be the worse case. Measurements reported in Fig. 2 (c) demonstrate a decreasing of 3dB in the ER with an optical input power weakening of 18dBm, which corresponds to an implementation of a 8x8 matrix structure.

The proposed scheme can work as a multi register matrix for n-bit packet buffering. In particular a packet can be stored in each specific memory cell and read after a time multiple of the packet time. Anyway synchronous operations are needed without the possibility to totally randomly access to the memory. The bulk realization of the scheme not allowed for reduced dimension of the loop, thus permitting only hundred of KHz operations. Anyhow, the photonic digital processing becomes more effective and attractive especially if it can be realised with integrated solutions. The use of SOAs in the scheme is attractive for their compactness, stability, low switching energy and low latency, as well as for the possibility of integration by hybrid solutions. By reducing the loop dimension to millimetres the processing of picoseconds bit could be possible, thus allowing for GHz digital photonic operations.

4. Conclusions

A novel scheme for a multi-cell ODRAM composed by independent 1-bit memory elements is proposed. The solution allows for optical and dynamic writing, reading and refreshing operation without any external synchronization. Each cell is based on a wavelength preserving SOA variable optical buffer. True dynamic random access functionality is firstly demonstrated for 1-bit memory element and the scalability toward a multi-cell ODRAM is then verified. The proposed scheme can work as a multi-register matrix for synchronous operation with n-bit packet. By photonic integration the bit time can be reduced up to picoseconds thus allowing for GHz digital processing.

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4. References

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