AC-coupled Reset-less 10 Gbps Burst-mode 3R Receiver Using an Internal Scrambling Scheme

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Abstract: We propose and experimentally demonstrate a fully AC-coupled reset-less burst-mode 3R receiver with a novel internal scrambling scheme for an easily-implementable 10Gbps PON-OLT. Fast acquisition time of 400 nsec is achieved without external control.
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1. Introduction

Broadband applications such as high-density video distribution are emerging and the passive optical network (PON) has been identified as the main technology to deliver such services. GE-PON [1] or G-PON [2] systems have been widely installed as fiber-to–the-home (FTTH), and next generation higher speed PON, 10G-EPON [3], was ratified in September 2009. In PON system, the burst-mode transmission technique is used for upstream (US) signal transmission, featuring a burst-mode 3R receiver (BM-3R-Rx) which captures bursty signals having different power and varying phase across bursts.

For PON systems, a low-cost architecture and a simple implementation method are required. One approach for achieving a low-cost architecture is to reduce the number of integrated circuits (ICs) by monolithic integration and AC-coupling. Besides, a simple control method is achieved by reset-less BM-3R-Rx. However, a conventional AC-coupled and reset-less BM-3R-Rx cannot receive a bursty signal with a short preamble after a long dark period.

In this paper, we propose an AC-coupled and reset-less BM-3R-Rx using a novel inter-chip signal transmission scheme, which we call "internal scrambling scheme" for fast acquisition to a bursty signal. Moreover, we demonstrate that the proposed architecture realizes a fast acquisition time of 400 nsec, which is significantly shorter than the IEEE 802.3av 10G-EPON specification: $T_{receiver\_settling} + T_{CDR} \leqq 1{,}200$ nsec.

2. Technical issues of conventional BM-3R-Rx

A BM-3R-Rx in an optical line terminal (OLT) consists of two parts: a burst-mode 2R receiver (BM-2R-Rx) [4] and a burst-mode clock and data recovery module (BM-CDR). At the OLT, there is also a large scale integration (LSI) of digital logic, including medium access control (MAC), which is connected to a BM-3R-Rx. If input and output signal amplitudes of CDR are sufficiently large, the CDR and logic circuit blocks can be suitable for integration into a single LSI circuit in complementary metal-oxide-semiconductor (CMOS) for low-cost OLT. On the other hand, since a BM-2R-Rx includes a large gain amplifier, which is based on an analog circuit, it is not suited for CMOS circuit implementation. An AC-coupling is the best solution to interface differently-processed ICs without a signal level conversion circuit. Moreover, it is becoming increasingly common to use AC-coupling as a high-speed IC interface. Two examples of this include XAUI [5] or CAUI [6].

The AC-coupling between a BM-2R-Rx and a BM-CDR must have large capacitance in order not to degrade the received signal via low-frequency cut-off. Since a large capacitance leads to slow burst response, the bandwidth-efficiency can become very limited. Such that an external control method is often used in order to settle the baseline drift quickly [7], however, the control signal is necessary to be served from the MAC to the BM-2R-Rx and the BM-CDR in the PHY layer. Even though the PHY input accuracy of external control signals should be on the order of several hundred ns, IEEE802.3 does not specify the control signal between PHY and MAC. Therefore, the crossing boundary between the layers of the control signal causes timing inaccuracy and interoperability issues. In addition, as long-reach PONs using optical-electrical-optical (OEO) conversion type reach extenders (REs) don't include a MAC, the solution would require reset-less operation.

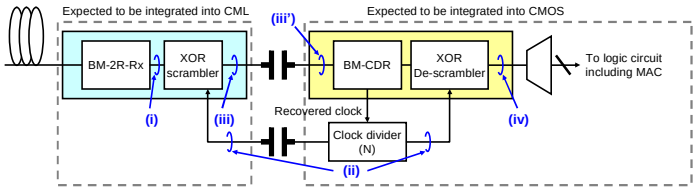
3. Proposed BM-3R-Rx using internal scrambling scheme

In order to achieve a fast acquisition time with an AC-coupled and reset-less BM-3R-Rx, we propose a novel internal scrambling scheme. Fig.1 shows a block diagram (Fig. 1a) and the waveform transformation process (Fig. 1b) of the proposed BM-3R-Rx. The BM-3R-Rx consists of a BM-2R-Rx, XOR-scrambler, BM-CDR [8] and XOR-De-scrambler. The BM-2R-Rx and the BM-CDR are both reset-less type, and the BM-2R-Rx also has a simple

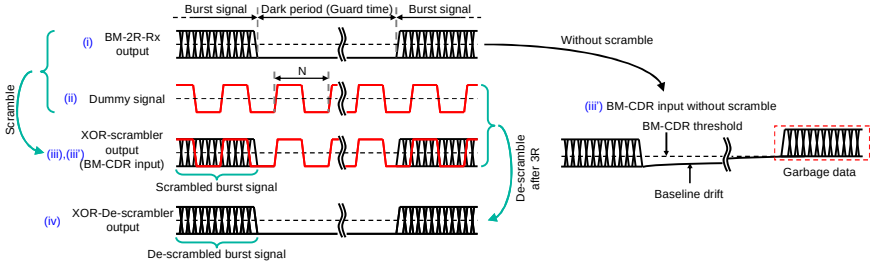
architecture with fast AC-coupling [9]. The XOR-scrambler and the XOR-Descrambler are expected to be integrated into each chip, BM-2R-Rx and BM-CDR (logic LSI) with a simple logic gate circuit in order to avoid interface mismatches. The BM-2R-Rx output signal is scrambled by the dummy signal with the XOR-scrambler, and de-scrambled at the BM-CDR output with the XOR-De-scrambler.

In order to synchronize the dummy signal with the burst signal automatically, the dummy signal is generated by dividing the recovered clock from the BM-CDR. In designing the proposed BM-3R-Rx, the clock dividing ratio (N) is one of the most important factors. At the head of a bursty signal, the dummy signal and the burst signal are not synchronized, because the BM-CDR takes some time to provide a clock signal synchronized with the burst signal. An unsynchronized signal due to the dummy signal in the XOR-scrambler output acts as phase-noise for the phase locked loop (PLL) in the BM-CDR. In a PLL circuit, a phase detector (PD) detects the phase difference between the input signal and the internal clock, and smoothes the detection result to drive the voltage controlled oscillator (VCO) [10]. Therefore, the clock dividing ratio (N) should be made large enough to prevent phase noise in the PLL circuit.

The proposed fully AC-coupled reset-less BM-3R-Rx can avoid the baseline drift at the AC-coupling with large capacitance between BM-2R-Rx and BM-CDR and garbage data shown as (iii') in Fig.1 (b), because the signal through the AC-coupling is scrambled during the dark period. Therefore, the PLL can start the clock synchronization to the burst signal at the beginning of the burst.



(a) Block diagram



(b) Waveform transformation process

Fig.1: Proposed BM-3R-Rx

4. Experiment and discussion

We carried out an experimental evaluation of the BM-Rx, with Fig.2 illustrating the block diagram of the setup. 10.3125-Gbps burst signals were generated by directly-modulated DFB-LD, with extinction ratios (ER) > 6 dB. The preamble pattern was an IEEE802.3av standard pattern. And the cut-off frequency of AC-coupling between the XOR-scrambler and BM-CDR was 7 kHz. We evaluated the preamble length and bit error rate (BER) characteristics by changing the clock dividing ratio (N) of the proposed BM-3R-Rx. Fig.3 shows the waveform of CDR input signal. The dark periods are scrambled by the dummy signal, no baseline drift is observed.

Fig.4 (a) and (b) show the BER characteristics comparison between a conventional and proposed BM-3R-Rx. The both BER characteristics satisfy the IEEE802.3av, PR-30 specification. Fig. 4(a) shows the burst-mode BER characteristics of a burst signal after 10 μsec dark periods. The preamble length was set to 200 nsec. The blue line (i) plots the BER with N=32, and the red line (ii) plots BER with N=16. Compared to continuous-mode BER with conventional BM-3R-Rx, (i) shows the burst signal was received without degradation. Meanwhile, (ii) demonstrates that degradation occurred because of the delay of clock recovery due to scrambling.

Fig. 4(b) shows the burst-mode BER characteristics after a loud burst signal, illustrating the general worst case for burst reception. The optical power of the loud burst signal was set to -6 dBm, the phase difference between the measured burst signal and the loud burst signal was 0.5 UI, and the guard time (time interval from the end of the loud burst to the head of measured burst) was 5 nsec. The clock dividing ratio was set to N=32, and the preamble length of the measured burst signal was set to 400 nsec. This is a longer preamble length than in Fig. 4(a) because about a 200 nsec-longer settling time is required after a loud burst signal than burst reception after a dark period due to time constant of AC-coupling in the BM-2R-Rx. The green line (iii) plots burst-mode BER after the loud burst signal, indicating that the 400-nsec preamble is sufficient to receive a burst signal in the worst case.

Fig.5 plots preamble length sufficient for receiving bursty signals without degradation versus the dummy pattern length (=N). As the dividing ratio N becomes larger, the required preamble length becomes shorter because the phase noise by the dummy signal becomes smaller. Compared to measurement with electrical signals, in measurement with optical burst signals and BM-2R-Rx, a longer preamble length was needed to avoid BER degradation due to the BM-2R-Rx settling time. Fig. 5 also shows that the preamble length to receive the burst signal in the worst case is less than 400 nsec for N $\geqq$32. Compared to the 1,200 nsec specification in IEEE802.3av, a 400-nsec preamble length is a 66.7% improvement.

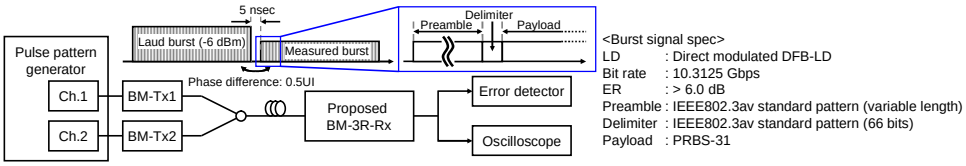


Fig.2: Experimental setup

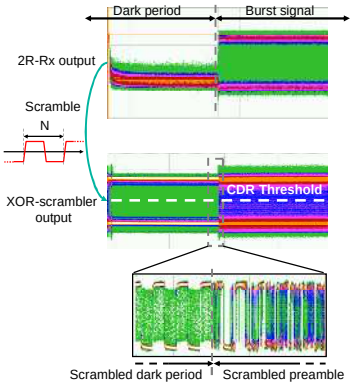
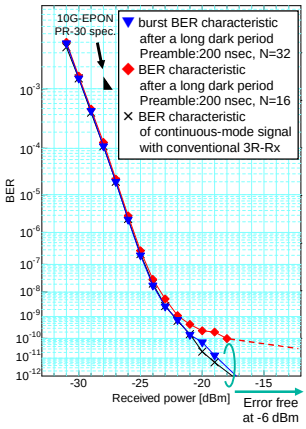
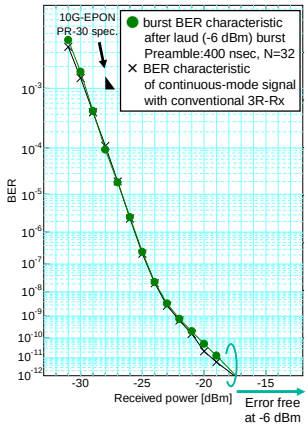


Fig.3: Waveform of CDR input with proposed BM-3R-Rx



(a) BER after 10 μsec dark period



(b) BER after laud burst signal

Fig. 4: BER characteristics with proposed BM-3R-Rx

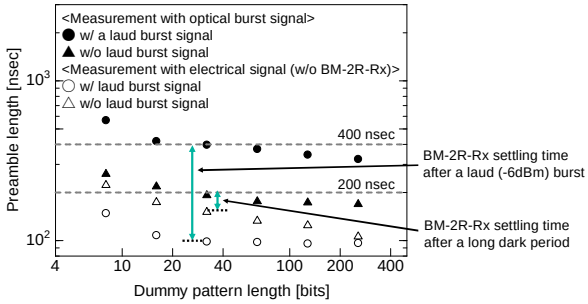


Fig.5: Preamble length sufficient for avoiding BER degradation versus Dummy patten length N.

5. Conclusion

A fully AC-coupled and reset-less BM-3R-Rx using a novel internal scramble scheme for 10 Gbps-class PON is proposed and experimentally verified. We demonstrated that the proposed BM-3R-Rx is free from baseline drift at the AC-coupling between the BM-2R-Rx and the BM-CDR by scrambling the BM-2R-Rx output. Moreover, we demonstrated the fast acquisition time of 400 nsec. This scheme can be applied to simple, easily-implementable BM-3R-Rx for 10Gbps PON-OLT.

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References

[1] IEEE802.3ah GE-PON, [2] G.984 G-PON, [3] IEEE802.3av 10G-EPON, [4] S. Kimura, et al., OFN/NFOEC2009, OWH6, [5] IEEE802.3ae-2002, [6] IEEE802.3ba-2010, [7] J. Sugawa, et al., ECOC2010, Mo.2.B.4 [8] F. Chang, ECOC2009, P6.29 [9] S. Takahashi, et al., OFC/NFOEC2010, OThE7, [10] Razavi B, "A 10Gb/s CMOS Clock and Data Recovery Circuit with Frequency Detection", Phase-Locking in High-Performance Systems:From Devices to Architectures, pp. 688 – 690, 2003