Progress in Soft-Decision FEC

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Abstract: We discuss the practical implementation of LDPC codes in soft-decision FEC for 100 Gb/s digital coherent systems. The question of the definition of net coding gain for differential QPSK used to avoid cycle slip is raised.
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1. Introduction

The transmission distance and speed in optical communications are primarily limited by optical signal-to-noise ratio (OSNR) and waveform distortion. The well established adaptive equalization algorithms being deployed with recent digital coherent technologies make possible a drastic improvement in the waveform distortion. However, no matter how good the equalization performance may be, it is never possible to restore the received OSNR once it has been degraded. Moreover, as the level of an M-ary modulation scheme increases, greater OSNR is required because the decreased Euclidean distance between each signal point in the constellation makes it more difficult to distinguish between the states. Only forward error correction (FEC) can compensate significantly for low OSNR. Addressing this issue is prompting an increasing demand for powerful FEC to reduce the required OSNR.

Recently, several trials aimed at exceeding a net coding gain (NCG) of 10 dB have been initiated. Chan *et al*. proposed a continuously interleaved BCH code having an NCG of 9.35 dB with 7% redundancy [1]. This is considered to be one of the best performing hard decision FECs for optical communications. On the other hand, soft-decision is a promising way to improve the error correction capability effectively. Thanks to the advent of digital signal processing (DSP) LSIs with high-speed analog-to-digital converters (ADC) for digital coherent systems, soft-decision decoding becomes much easier to incorporate into the receiver hardware. In response to this trend, Miyata *et al*. proposed soft-decision triple-concatenated FEC using low-density parity-check (LDPC) codes with an NCG of 10.8 dB at 20.5% redundancy [2]. They verified its performance by implementing the entire 100 Gb/s circuit on FPGA emulators. Xie *et al*. presented a soft-decision LDPC(18353,15296) code with an NCG of 11.28 dB at 20% redundancy [3]. A longer codeword brings with it increased NCG and also prevents any unwanted error flaring floor.

In this paper, we discuss how soft-decision FEC is becoming practical in digital coherent receivers using high speed ADCs. LDPC codes are introduced as good candidates for strong soft-decision based FEC. Several implementations of soft-decision LDPC codes are considered for 100 Gb/s transmission, where error floor is a critical issue needing to be addressed. To overcome this, the concatenation of hard-decision FEC and soft-decision based LDPC codes is proposed to achieve more than 10 dB NCG compliant with Optical Internetworking Forum (OIF) standards. In the last part, we raise an important question for the definition of NCG in digital coherent systems with and without differential QPSK coding, which is generally used to avoid phase slip caused by the practical limitations in processing the phase recovery algorithms.

Note that the NCGs presented in this paper are defined at a post-FEC bit error ratio (BER) of 10^{-15}.

2. Soft-Decision FEC

Soft-decision decoding uses not just the conventional '1' vs. '0' decision but also an indication of how certain we are that the decision is correct. Fig. 1 illustrates a typical soft-decision structure for a QPSK constellation. The 2^N-1 decision thresholds sandwiched between the two signal states of the in-phase and quadrature phase components are used for soft-decision decoding. In the case of N = 3, the two possible received signals, '1' and '0', lie in regions represented by a binary vector ranging from [011] to [111]. The left-most bit is the hard-decision digit, and the other two digits are information bits indicating the probability of '1' or '0'.

Conveniently, a recent digital coherent receiver has an ADC at its front end for demodulating the multi-level coded signals. This suddenly makes it much easier to realize soft-decision decoding, even though the bit rate is much higher than previously. The coding gain can in principle be improved by $\pi/2$ by using soft-decision decoding with infinite quantization bits N and redundancy, an approximately 2 dB difference. In a practical implementation of QPSK, an N of 4 is sufficient to obtain near ideal error correction performance.

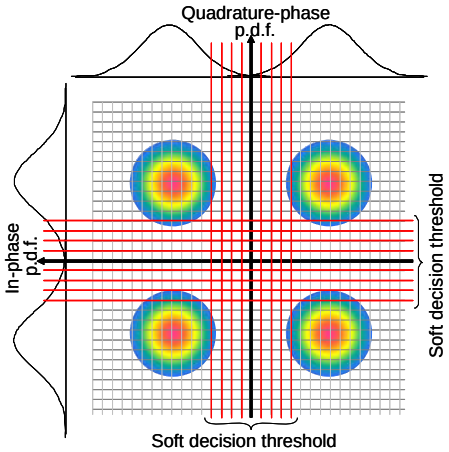


Fig. 1 Typical 3-bit soft decision for QPSK signal

3. LDPC Codes

For 100 Gb/s optical communications, one potential candidate for strong soft-decision based FEC is an LDPC code, a linear code defined by the sparse parity-check matrix invented by Gallager, which is expected to exhibit superior error correcting performance. Studies into applying LDPC codes to optical communications were instituted as early as 1999 by Djordjevic *et al*. [4]. The expected merits of LDPC codes are not confined to high error correction capability, but also fit them for parallelization to reduce circuit complexity. In an LSI for high speed optical communications, ease of parallelized signal processing is essential for practical implementation.

Fig. 2 illustrates four types of FEC frame structure and associated transponder configuration for a 100 Gb/s digital coherent system, which each consist of an OTU4 framer LSI, a coherent ASIC and an optical front-end. The FEC redundancy is assumed to be 20% as recommended by the OIF. The OTU4 framer LSI transforms the 100GbE signal to and from the OTU4 framed format, and usually incorporates a hard-decision FEC, *e.g.* RS(255,239) plus concatenated codes per ITU-T G.975.1. The coherent ASIC includes an ADC and DSP for received signal quantization, dispersion compensation, phase estimation, clock recovery, polarization de-multiplexing, and adaptive equalization of waveform distortion due to polarization mode dispersion.

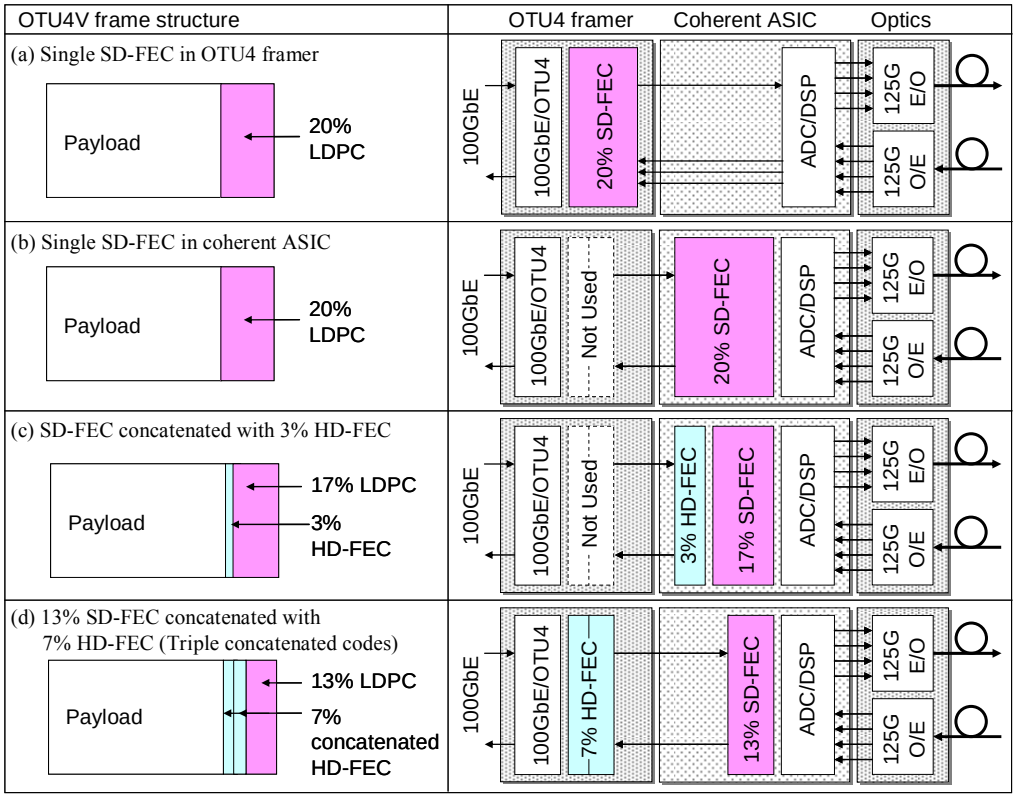


Fig. 2. Four types of FEC frame structure and optical transponder for a 100 Gb/s digital coherent system

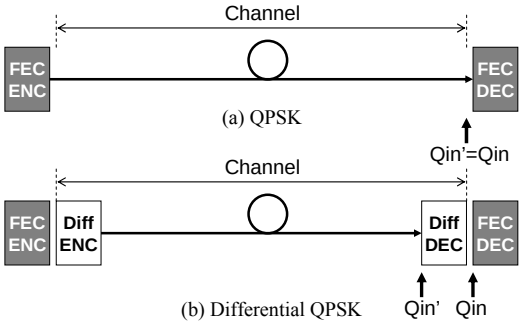
In Fig. 2(a) and 2(b) a single 20% LDPC code is implemented in respectively the OTU4 framer or the coherent ASIC. It is expected that the 20% redundancy of the LDPC code will provide superior error correction performance. However, in order to suppress the unwanted error floor which is inherent to LDPC codes, a very long codeword is required. This results in a large circuit and high latency. Fig. 2(a) has the drawback that a huge interconnection speed at N+1 times the transmission rate is needed between the OTU4 framer LSI and the coherent ASIC, *e.g.* for N=3, a 125 Gb/s x 4=500 Gb/s interconnection is required. Fig. 2(c) shows another way to easily eliminate the LDPC code error floor. The error floor of the inner soft-decision (SD)-FEC in the coherent ASIC is suppressed by concatenating it with a weak 3% outer hard-decision (HD)-FEC code. Under this concept, the concatenation of LDPC(9216,7936) and RS(992,956) codes has been experimentally demonstrated to show an NCG of 9.7 dB (= 9.0 dB at 10^{-13}) with only 2-bit soft-decision and 4 iterations [5]. Fig. 2(d) is thought to be the most practical implementation. An SD-FEC with a relatively short codeword and small circuit is implemented in the coherent ASIC as the inner code, concentrating on the higher BER ($>10^{-3}$) region. The inevitable increase in the residual BER floor is cleaned up by the concatenated HD-FEC in the OTU4 framer LSI. This concept was given the name "triple-concatenated FEC" [2]. FPGA emulation verified that concatenated LDPC(4608, 4080) and G.975.1 codes achieve an NCG of 10.8 dB with 20.5% redundancy.

4. FEC in Differential QPSK

In digital coherent transmissions, realistic linewidth, additive noise, and unwanted nonlinearity interaction cause catastrophic failure due to cycle slips more often than expected [6]. The phase estimate becomes incorrect over a quarter cycle, and stays wrong indefinitely. When a cycle slip occurs, at least one OTU frame (4080x8x4 bits) is lost. In order for the burst error correction capability of the FEC to be able to recover this, an impossible interleaving depth of at least 100 OTU frames would be necessary. Instead, differential QPSK is usually employed, in which a cycle slip causes 2 consecutive errored bits. The BER of differentially encoded QPSK is $2p(1-p)$, where p is the error probability of synchronous detection QPSK, which is equivalent to an OSNR penalty of 1.1 dB at around 10^{-2}.

Fig. 3 shows simplified block diagrams for (a) QPSK and (b) differential QPSK. The received Q can be defined at two points. Qin is the FEC decoder input Q. Most systems are defined in terms of this. The input Q of a differential decoder is Qin'. Most optical engineers consider this point to be the receiver input. Note that the definition of Q here is a simple conversion from BER using *erfc*. Fig. 4 illustrates the difference in FEC performance of QPSK and differential QPSK. The SD-FEC is assumed to be the triple-concatenated FEC using LDPC codes type [2]. The Q difference between uncoded QPSK and uncoded differential QPSK is just 0.09 dB at 10^{-15}. With decreasing Qin', the difference widens, *e.g.* to 1.07dB at $2x10^{-2}$. The NCG for QPSK is calculated to be 18dB-6.4dB+10log(1/1.2)=10.8dB. In contrast, the NCG of differential QPSK appears to be 18dB-6.4dB-1.07dB+0.09dB+10log(1/1.2)=9.8dB. Is the NCG really degraded? The answer is no. The reason why the NCG looks degraded is that the Qin' difference between QPSK and differential QPSK is different at different corrected BERs, *e.g.* 0.09 dB at 10^{-15} and 1.07dB at $2x10^{-2}$. The inherent performance of the FEC will not be degraded as long as the FEC can correct up to 4-bit short bursts.

When trying to design a system power budget to ITU-T G.977, the 1.07dB degradation due to differential coding should be included in the mean Q value (in Fig. 3, use Qin not Qin'). A Q limit of 6.4 dB should always be used.



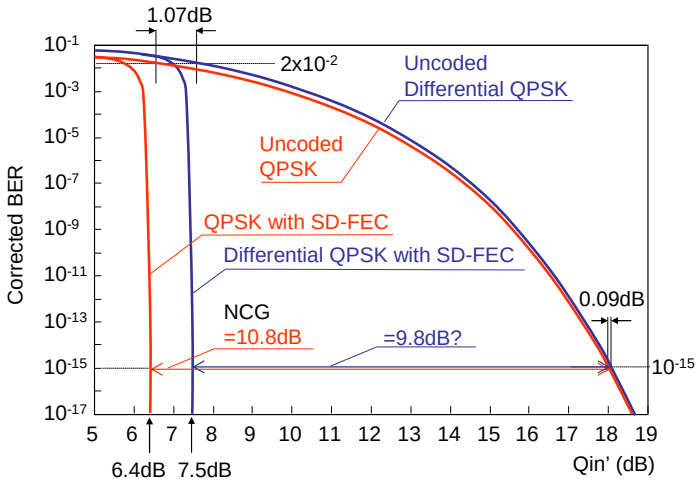


Fig. 3. Simplified block diagrams of (a) QPSK and (b) differential QPSK Fig.4. Soft decision FEC performance of QPSK and differential QPSK

5. Conclusions

We reviewed recent progress in soft-decision FEC for optical communications. LDPC codes are expected to be strong candidates for soft-decision FECs. We showed and compared four ways of implementing LDPC codes in OTU4 framer LSIs and coherent ASICs. A triple-concatenated FEC is introduced as one of the strongest soft-decision FECs for 100 Gb/s transmission. We also discussed the definition of NCG in digital coherent systems with and without differential coding, which latter is generally used to avoid phase slip caused by the practical limitations in processing the phase recovery algorithms.

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