First demonstration of OPS and burst detection of 160 Gb/s packets through three 52 km-spaced optical nodes

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Abstract: We demonstrate error-free transmission, dynamic switching and burst detection of 160Gbps packets with guardtime ~1ns through 3-nodes that include on-the-fly optical packet switching and instantaneous locking/unlocking time clock extraction subsystems.
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1. Introduction

The exponential growth of the traffic in the access networks makes it likely that future optical metro and core networks should be capable to handle tens of Tb/s data traffic [1, 2]. It is therefore envisioned that optical links that interconnect the optical node of the network will carry optical packets at data rates above 100 Gb/s. Assuming 160 Gb/s packets with typically 1000 bytes, the length of each packet would be around 50 ns. In order to optimize the load at which such a system can operate the guard times between the packets have be small (in the order of a few nanoseconds). This requires that the system has a fast node controller that recognizes the packets destination and sets the optical switches within a few nanoseconds. Short guard time also require a receiver with a packet based clock extraction circuit with very fast (also within a few ns) locking/unlocking time to implement optical time demultiplexing and data burst reception at 160 Gb/s.
Despite a few solutions for a fast label processor capable of handling data packets at 160 Gb/s [3-5], transmission and packet based clock extraction with a very fast locking/unlocking time was only demonstrated up to 40 Gb/s [6].
Therefore, up until now, to the best of our knowledge, a transparent optical node with a nanosecond switching time for 160 Gb/s data packets has never been demonstrated and verified in a transmission system.
Here we present for the first time a transparent optical node that includes an asynchronous and optical packet switch sub-system and a packet based clock extraction for data burst detection of 160 Gb/s data packets. We present transmission and dynamic packet switching of 160 Gb/s data packets (single wavelength) through three nodes with a transmission span of 53 Km. The on-the-fly operation of the optical packet switch and the instantaneous locking/unlocking times of the clock extraction allow very short packet's guard-times of 1 ns.

2. System operation

Figure 1 shows the transmission system and the schematic of the optical packet switch. To test the fast operation of the optical packet switch and packet clock extraction, we generate 6.4 ns short data packets.
The packet payload is generated by time-quadrupling a 40 Gb/s data packet (λp=1549.8 nm) containing 255 bits (2^8-1 PRBS pattern) to obtain a 160 Gb/s data packets with 1024 return-to-zero bits using a passive fibre-based pulse interleaver. This results in a short packet payload of 5.4 ns data burst with a guard-time between the packets of around 1 ns. Each pulse has duration of 1.5 ps making the 20 dB optical bandwidth of the payload to be 5 nm. We exploit this wide optical spectrum of the OTDM signal to insert in-band a 10 GHz clock pilot and the labels (see spectrum of the packets in Fig. 1). The approach to insert a clock pilot spectrally in-band with the packet payload was investigated before, only in a back-to-back configuration with no transmission [7]. In this work both the clock pilot and the packet address are packetized together with the payload and transmitted through the optical nodes. This leads the payload, clock, and address to experience the same dispersion-dependent impairments. Moreover, the clock pilot and the addresses can be asynchronously extracted by passive wavelength filtering and processed, while the payload remains in the optical domain. The burst 10 GHz clock pilot at 1552.52 nm is combined with the payload and the address through an optical coupler. To improve the phase noise of the clock pilot, a portion of the payload spectrum where carved by a fiber Bragg grating (FBG1) centered at 1552.52 nm with a 3 dB bandwidth of 0.4 nm and 30 dB suppression of the rejection band.
The packet address is encoded with cw-signals (labels) at wavelengths within the 5 nm payload bandwidth and duration equals to the payload length. Each label has a binary value: '0' means no signal at the label wavelength, '1' means an optical signal at the label wavelength. Thus, 2^N addresses can be encoded by only using N in-band labels.

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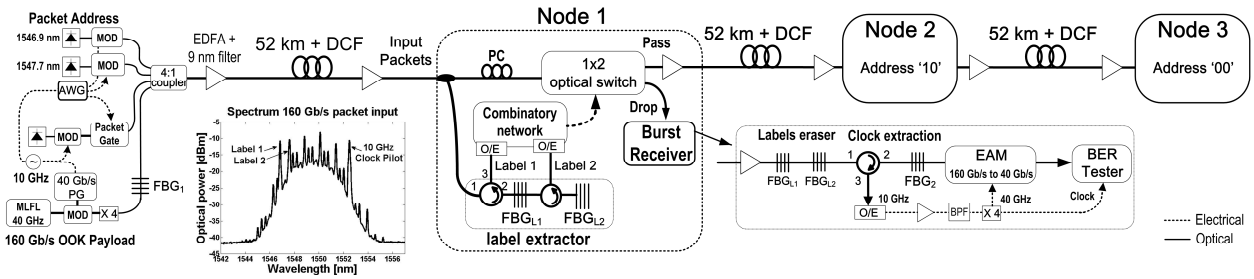

Fig. 1: Experimental set-up. MLFL: mode-locked fiber laser, AWG: arbitrary waveform generator, PG: pattern generator, O/E: optical-to-electrical converter, PC: polarization controller, DCF: dispersion compensation fiber.

We have demonstrated in [3] packets with up to 6 labels, which can address up to 64 nodes. Here we use two in-band labels at λL1=1546.9 nm and λL2=1547.7 nm to encode 4 addresses that identify the three optical nodes in the system.

At each optical node the power of the packets is split by a 90:10 coupler. 90% of the power is fed via a polarization controller into the 1x2 electro-optic switch based on LiNbO3 technology. The 10% of the power is fed into the label processor. In the label processor, the labels are extracted by cascading two FBGs centered at the labels wavelengths and two optical circulators. The FBGs have Gaussian profile with 98% of reflectivity and 6 GHz at -3dB bandwidth to avoid significant slicing of the payload spectrum that might lead to distortions. The parallel labels are detected and processed by the electrical combinatory network. Very low speed, cheap, and low sensitivity detector can be employed to detect the low speed labels. The combinatory network processes asynchronously and on the fly the parallel labels and can be scaled for larger number of labels without increasing the latency. This leads to a packets guard-time of 1 ns. The combinatory network provides the control signal of the 1x2 electro-optical switch. According to the encoded address, the packets are then forwarded to the next node or dropped and received.

The burst receiver consists of a packet clock extraction and an 160 Gb/s to 40 Gb/s time demux. First, the labels are erased by using a copy of the FBGs employed in the label processor. Then the payload and the 10 GHz clock pilot are separated via an optical circulator and FBG2, which is identical to FBG1. This allows fast-locking/unlocking times; locking is realised every time a packet arrives at the receiver and unlocking occurs when the packet ends. The history of the previous packet is completely forgotten when the next packets arrive. As the clock and payload are transmitted synchronously and are spectrally in-band, they are affected by the same impairments leading to the same phase drifts. Thus, the relative phase between the clock and the data is preserved. The 10 GHz extracted clock is converted to the electrical domain by a photodetector, amplified and correspondingly quadrupled (× 4) to drive the 40 GHz electro-absorption modulator (EAM) to time demux the 160 Gb/s data to 40 Gb/s data. This allows the 40 Gb/s data to be analyzed by commercial BERT system.

3. Experimental results

The experimental set-up to test the transmission and dynamic switching of the 160 Gb/s packets is shown in Fig. 1. The system consists of three nodes with a transmission span of 52 Km of true-wave reduced slope with carefully chromatic dispersion compensation and amplification and filtering at the fibers output to restore signal fidelity. Each node is identified by an address. Optical packets with different addresses are launched in the system (see Fig. 2 (a-c)). Each node let pass or drop the packets according to the packet address. Figure 2 shows the dynamic switching operation of the optical nodes. The control signal generated by the combinatory network provides 6 Vpp to drive the 1x2 optical switch is shown in Fig. 2d. Figures 2(e-f) show the dropped (packet address '10') and passed packets at node 1. The contrast ratio between the dropped and transmitted packets was 18 dB. Similarly, Figs. 2 (g-h) show switching signal and the dropped packets with address '10' at node 2. The packets with address '00' are detected by the node 3 and are shown in Fig. 2i. Open eye diagrams, recorded by using the extracted clock at each node, are clearly visible in Fig. 3. To hold the persistence of the clock, we have filtered the clock with a 10 GHz electric filter with 10 MHz bandwidth. The phase noise of the extracted clock is reported in Fig. 4. The integration of the noise spectrum reveals a timing jitter lower than 90 fs with only slightly increase after 160 Km of transmission. The extracted clock was quadruped to drive the 160 Gb/s data to 40 Gb/s data demux, and to clock the BERT tester. The best case (filled symbol) and worst case (half-filled symbol) BER curves recorded for the switched packets at each node are reported in Fig. 5. As reference we report the BER curve of the back-to-back (b-t-b) payload. Error-free operation with 0.65 dB, 1.6 dB, and 3 dB of penalty was measured at node 1, node 2, and node 3, respectively. This penalty is attributed to the carving effect of the FBG and the accumulated ASE noise.

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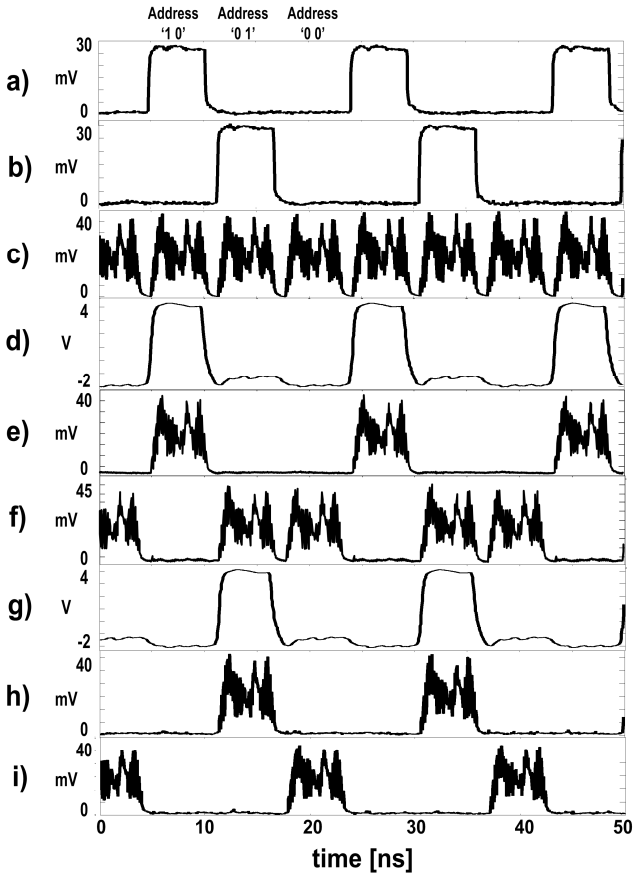

Figure 2. Measured traces.
a-b) Labels of the input optical packets;
c) Input packet payload;
d) Control signal generated by node 1;
e-f) Packets dropped and passed at node 1;
g) Control signal generated by node 2;
h-i) Packets dropped and passed at node 2.

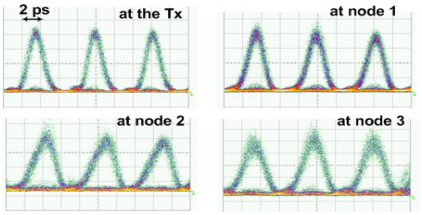

Figure 3. Eye diagrams at different optical nodes.

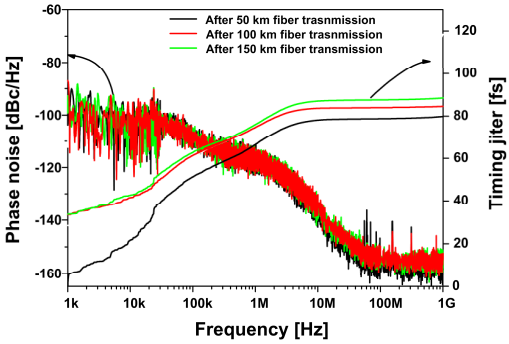

Figure 4. Phase noise and timing jitter of the extracted clock. at different optical nodes.

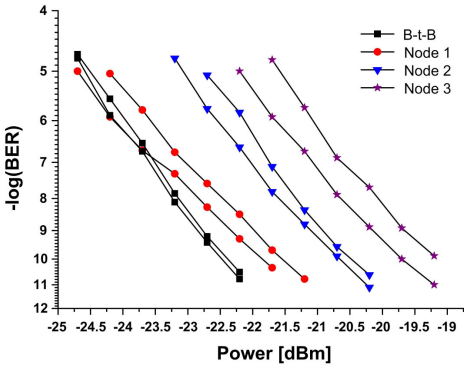

Figure 4. BER curves at different optical nodes.

3. Conclusions

We have demonstrated error-free transmission, dynamic switching and detection of 160 Gb/s data packets through three optical nodes. The on-the-fly operation of the packet switch and the instantaneous locking/unlocking times of the clock extraction allow very short packet's guard-time of 1ns. This is essential to effectively speed up the optical network. Error-free operation with 3 dB penalty and a phase noise of the extracted clock lower than 90 fs were measured after three nodes. Those results, and the capability of the proposed technique to process a large number of addresses, indicate that systems with larger amount of nodes and longer transmission lengths are feasible.

4. References

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