Realization of a 23.9 Gb/s Real Time Optical-OFDM Transmitter with a 1024 Point IFFT

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Abstract: We report a FPGA-based real time 23.9-Gb/s CO-OFDM transmitter with IQ-mixing with a 1024 point FFT, the largest FFT-size reported to date. For a BER of 10^{-3} a required OSNR of 10.8 dB is measured.

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1. Introduction

Orthogonal frequency division multiplexing (OFDM) has emerged as a promising modulation technique in the field of optical communications. Coherent optical OFDM (CO-OFDM) is one of the modulation formats that have been proposed to overcome limitation due to linear transmission impairments such as chromatic dispersion (CD) and polarization mode dispersion (PMD) [1, 2]. Until recently most of the CO-OFDM transmission experiments are realized by storing floating point transmitter data into arbitrary waveform generators (AWG).

An AWG is a good tool to investigate the transmission performance of OFDM for fiber-optic applications [3, 4] and can be used as transmitter for the realization of a real time receiver [5, 6]. However, a floating point transmitter is not as realistic as an ASIC or FPGA typically uses limited number of bits for processing. Therefore, the realization of a real time OFDM transmitter is essential for understanding the limits of realistic digital signal processing (DSP) algorithms.

Recently, several real-time OFDM experiments have been reported at ~10-Gb/s. Focusing on access applications, Giddings reported an 11.25 Gb/s real-time transmitter in [7] using a directly modulated laser. In this experiment a 64-QAM constellation size was used to realize 11.25-Gb/s real-time transmitter in a 1.9-GHz bandwidth. For long-haul fiber-optic applications Benlachtar et al. [8], reported a 8.36 Gb/s real time transmitter with a 4QAM constellation size. In this realization a 128 point inverse fast fourier transform (IFFT) was used to generate the OFDM signal. Buchali et al. [9], realized a 12.1 Gb/s transmitter with a 4QAM constellation size. In this experiment an IFFT-size 256 was used for the generation of the transmitter data. These studies show that the real-time CO-OFDM transmitters have restricted capabilities due to the limited resources of FPGAs. Therefore it is crucial to investigate in efficient VHDL algorithms that make it possible to overcome resource limitations.

In this work, we realize a real time CO-OFDM transmitter with a 1024 point IFFT at a data rate of 23.9 Gb/s. In this realization two FPGAs are synchronized and an IQ modulator is used for the modulation of the OFDM signal. Similar to [9] the IFFT is implemented on the Xilinx Virtex 5 platform. The constellation size is 4QAM and in back to back configuration, the required OSNR for a BER of 10^{-3} is 10.8 dB. Compared to the AWG operation of the DACs this has a penalty of about 0.1 dB.

2. FPGA based Transmitter

Fig. 1 depicts the block diagram of our real time transmitter with the back to back optical link. For the realization of the real time OFDM transmitter two FPGAs (XC5VFX200T) have been used to create the in-phase and quadrature data stream. Each FPGA is connected to a DAC board with 24 Rocket I/Os of 6.25 Gb/s each. On the DAC board four groups of 6 bit each are built from the 24 inputs and then 4:1 multiplexed in order to form a stream of 25 GSamples/s. In order to synchronize the DAC boards, they are fed with a 25 GHz clock. In addition, one of the DAC boards divides the 25-GHz clock by 128 internally to provide a reference clock to the two FPGA boards. The pre-processed data is read from ROM tables inside the FPGA, fed through the IFFT, afterwards clipped, and cyclic prefix is added. The real and imaginary parts are reorganized so that they are one after another in order to get a real output stream for DACs, parallel to serial converted and forwarded to DACs. The IFFT implementation will be further discussed in detail in Section 3. DAC outputs are amplified and fed to an IQ modulator. The laser used at the transmitter and receiver are ECL lasers with a linewidth of ~100 kHz. The output of the OFDM transmitter is fed to a noise loading stage. At the receiver, coherent detection is realized with a 90 degrees hybrid and two balanced photodiodes. After coherent detection offline processing is used including laser phase noise equalization, synchronization, sampling frequency offset compensation, and channel equalization with training symbols [10].

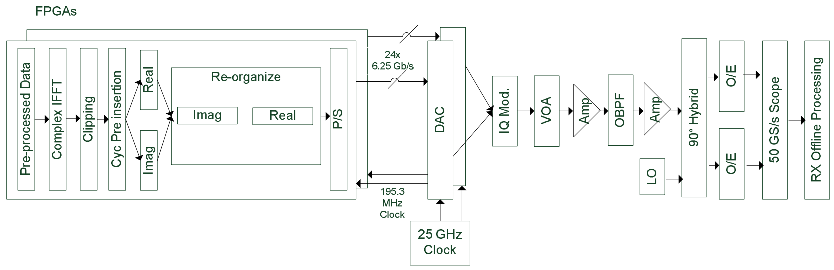

Fig 1. Real time transmitter and optical back-to-back link

3. IFFT Implementation

Ideally a single FPGA board would be used to compute IFFT and feed the two DACs where one DAC transmits the real part of OFDM signal, the other one the imaginary. However because of the limited number of high speed connections the FPGA and DAC boards have, it is not possible to realize an OFDM system with one FPGA board. In addition FPGA resources are too small. Therefore we choose in this design to realize the IFFT with one FPGA for the I and Q part respectively, a real valued IFFT has to be used in real time implementation for each DAC board. An efficient way of using a real valued IFFT is to compute two real-valued IFFTs with one complex valued IFFT [11, 12]. In order to achieve a real valued IFFT the input must satisfy the Hermitian symmetry condition

$$Y_{N-n} = Y_n^* \qquad (1)$$

for $n = 1, 2,\ldots, N$-1 and $\mathrm{Im}\{Y_0\} = \mathrm{Im}\{Y_{N/2}\} = 0$, where $\mathrm{Im}\{\cdot\}$ denotes the imaginary part, N is the number of IFFT points and Y is the complex data. So, if two Hermitian symmetric symbols are orthogonally summed, $Y(k)+jY(k+1)$, and passed through a complex valued IFFT, the result is $s^{y(k)} + j\, s^{y(k+1)}$, where $s^{y(k)}$ and $s^{y(k+1)}$ are both real valued and correspond to the IFFT's of $Y(k)$ and $Y(k+1)$, respectively. Consequently, $s^{y(k)}$ and $s^{y(k+1)}$ can be sent one after another to the DAC output.

At the transmitter, the random data is 4-QAM mapped. A gap is inserted in the middle of spectrum for the RF-pilot laser phase noise compensation technique [13]. The payload is concatenated with the training symbols whose peak-to-average power ratios (PAPR) is minimized so that nonlinearities do not degrade the performance of channel equalization at the receiver. The concatenated data are decomposed into $Y+j\,Z$ where both Y and Z are Hermitian symmetric [11]. Afterwards, Y and Z are processed separately by the two FPGAs. Since IFFT is a linear transform,

$$\mathrm{IFFT}(I) = \mathrm{IFFT}(Y) + \mathrm{j}\ \mathrm{IFFT}(Z), \qquad (2)$$

where I is the concatenated data. In other words, after IQ modulation, the preprocessed data embedded into two FPGA boards would give the same result as performing an IFFT on I.

The 1024 point IFFT and cyclic prefix addition takes place in the FPGA. Virtex 5 logic parts are able to operate at 400 MHz, however as more chip resources are used, the practical operating frequency decreases. The main advantage of using a complex IFFT to compute two real-valued IFFTs is that the DSP can be reduced to half the sampling rate (12.5 GHz instead of 25 GHz). We chose the degree of parallelization as 64 which results in a 195.3 MHz operating frequency. The IFFT uses decimation in time radix 2 algorithms and all twiddle factors are 8 bits. The input data to the IFFT is 5 bits. Each stage of the IFFT increases the number of bits by 1 due to additions and for all of the multiplications from the first stage to 10 one extra bit is added. As the 1024 point IFFT has 10 stages, this results in a total of 16 bits. However, as the DACs have a resolution of 6 bits, 10 bits must be discarded. The DSP uses 82% of DSP48E, 11% of block RAMs, 83% slice registers and %70 slice look up tables, one phase locked loop and one digital clock manager.

4. Experimental Results

In order to verify the optical performance of the real time CO-OFDM transmitter, a back to back performance evaluation was conducted. In this experiment the following parameters were used; 490 subcarriers out of 1024 are 4 QAM modulated and 64 samples of cyclic prefix are added to each OFDM symbol. 20 subcarriers in the middle of the spectrum are unmodulated in order to spare a gap for RF-pilot compensation. The rest of the subcarriers are used for oversampling. Two training symbols are sent every 40 payload symbols. As a result, the nominal data rate is

23.9 Gb/s, taking 7% FEC into account and the overhead for cyclic prefix and training symbol this results in a net data rate of 20 Gb/s. Fig. 2(a) shows the OFDM spectrum at the output of IQ modulator. The aliasing products due to DAC are visible at both sides of spectrum. Optionally LPFs can be used to eliminate these spectral components. Moreover, a pre-equalization function can improve the frequency roll-off of higher frequencies. The constellation diagram of the real time transmitter at high OSNR is depicted in the inset of Fig 2(b). In this constellation diagram the effects of residual laser phase noise and quantization noise are clearly visible. Fig. 2(b), in which for all measured points a minimum of 2 million bits are evaluated, shows the required OSNR for a BER of 10^{-3}. In this figure a comparison between real time transmitter and AWG is also made where FPGAs are utilized as AWG. In summary the required OSNR for the real time transmitter at BER of 10^{-3}, is 10.8 dB whereas it is 10.7 dB for AWG case. As the BER decreases, the difference increases. An error floor of 10^{-6} is observed due to the limited vertical resolution of DACs.

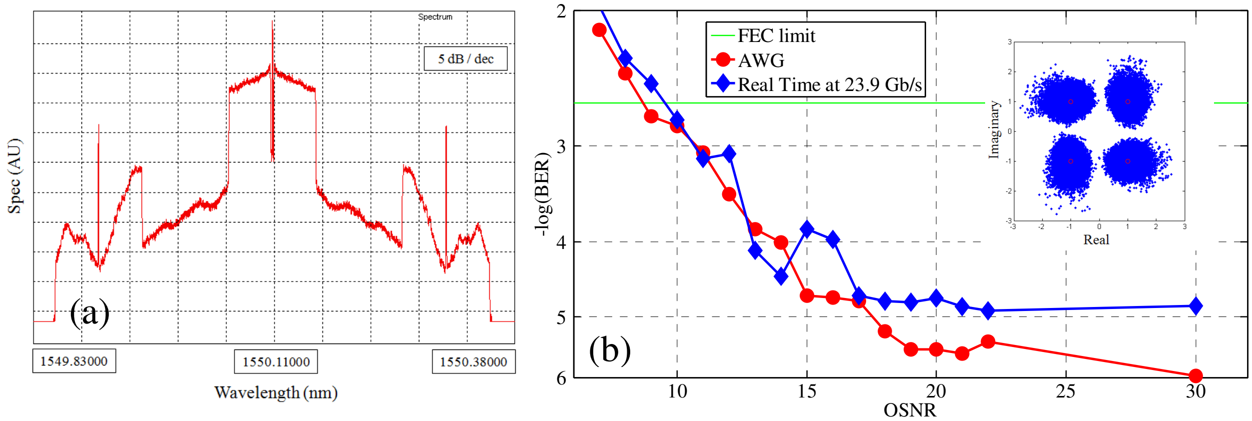

Fig. 2. (a) OFDM Spectrum, (b) Required OSNR performance in back-to-back configuration., (inset) Constellation diagram of the real time transmitter at 30 dB OSNR

5. Conclusion

We have demonstrated a real time OFDM transmitter with the highest IFFT size to our knowledge. We were able to realize 23.9 Gb/s with IQ mixing with a required OSNR of 10.8 dB for a BER of 10^{-3}. Compared to using the DACs as an arbitrary waveform generator a negligible implementation penalty was found for BERs above 10^{-4}.

6. References

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