All-optical RAM Buffer Subsystem Demonstrator

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Abstract: A comprehensive R&D program aiming at all-optical RAM buffer subsystem for optical packet switching will be presented, featuring nano-cavity based optical bit memory, a unique beam addressing optics, and optical SP and PS converters.
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1. Introduction

Green ICT is currently an emerging issue, and given an explosive growth of the Internet traffic, the power consumption of ICT will increases at the annual growth rate of around 5%. There are two main driving factors for the increasing power consumption; one is IP router at edges and core networks, and the other is optical network units (ONUs) in FTTH systems in the access network.

One of promising solutions to "Green Router" would be an optical packet switch. Key building blocks of packet switch are switchws, buffers, and the header processor. Recently, a prototype of hybrid optoelectronic router using electronic static RAM as the buffer, has demonstrated low power consumption at 10Gbps [1]. Further reduction of power consumption can be expected with all-optical packet switch. For the optical buffers, optical delay line and slow light devices without random access capability have been only choices, but the non-RAMtype of buffering severely limits the switching performance. To realize optical RAM buffer, an optical bit memory will be a key element. There have been studies on laser diode-based optical bistable device, but they are bulky and power-consuming.

In this talk, a challenging five-year-long government-supported R&D program since 2006 [2], aiming at energy-efficient, high-speed all-optical RAM buffer subsystem will be introduced. It will be shown that the targeted performance of key building blocks such of all-optical RAM buffer subsystem are achieved, including a nanocavity based optical bit memory, a beam addressing optics, and optical serial-to-parallel / parallel-to-serial converters for interfacing with an in/output time-serial optical packet. The low power consumption as well as low packet drop ratio within the constraint of small capacity and short memory holding time of the buffer will be discussed. Finally, write-in and read-out of this prototype RAM buffer demonstrator will be presented on site for the first time.

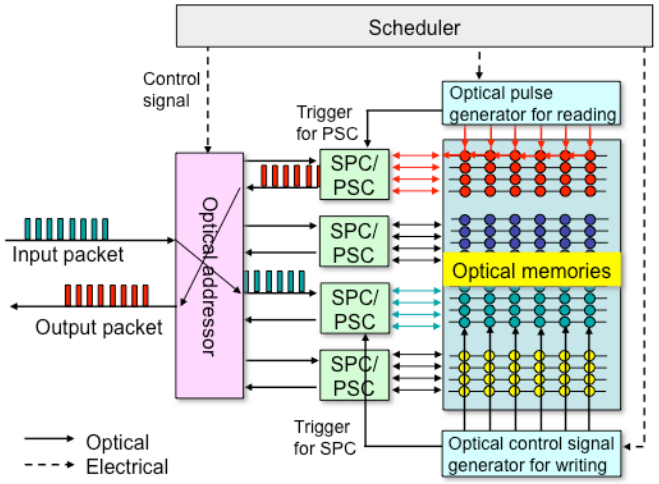

Fig.1 Architecture of all-optical RAM buffer subsystem

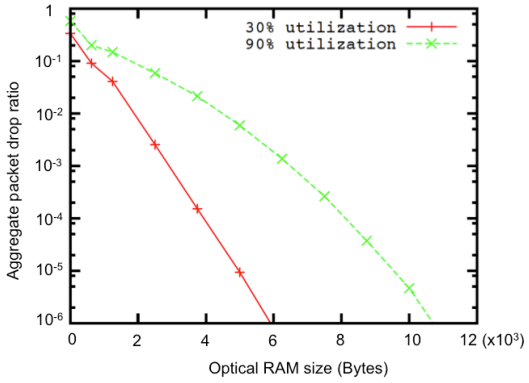

Fig.2 Packet drop ratio vs. buffer size

2. Quest for all-optical RAM buffer

An architecture of all-optical RAM buffer subsystem is illustrated in Fig.1. It consists of an array of nanocavity-

based optical bit memory devices, an optical addressor, and optical serial-to-parallel / parallel-to-serial converters for interfacing with an in/output time-serial optical packet.

Current buffer capacity required for electronic router will be too large for the limited capacity of all-optical RAM buffer. The performance of optical packet switch adopting all-optical RAM buffer with a limited capacity and holding time of the memory is theoretically analyzed. We have proposed optical rate-based paced XCP, which is a modified version of XCP enabling an intra-domain traffic shaping and congestion control protocol [3]. It is specially designed for WDM OPS networks with pacing at edge nodes for minimizing the buffer requirements at core nodes. NSFNET network is used for the simulation, having the total of 28 nodes (14 core nodes+14 edge nodes) and 35 links (21 core links+14 edge links). Edge nodes apply electronic buffering, but core routers use only all-optical RAM for buffering. All switches employ output buffering and cut-through bit-synchronized switching. It is assumed that there is a backlogged traffic at edge buffers, so each edge node sends traffic to all other edge nodes at the maximum possible rate controlled by XCP. The capacity of the data wavelength is set at 1Gbps. 60% of the packets are 40Bytes, and 40% of the packets are 1500Bytes. Fig. 2 shows the packets drop ratio in NSFNET topology vs. the buffer size under the output link utilizations of core routers at 30% and 90%. It can be seen that a low packet drop ratio can be achieved with buffer capacity of a few thousands of bytes, equivalent to to several 12kByte-long Ethernet packets. This is encouraging because the required capacity is realistic for all-optical RAM buffer.

3. Key building blocks

3.1 Photonic-crystal nanocavity-based optical bit memory

In order to realize all-optical RAM buffer, optical memories should be small, integrable,, low-power consumption, and long holding time, which are tough requirements for conventional photonics. To solve these problems, we have adopted memories based on photonic crystal nanocavities with the mode size of approximately 0.1 μm^3. The photonic band gap enables ultra-strong light confinement, which leads to extreme reduction of the operation power. In 2005, we reported a-proof-of-principle demonstration employing Si photonic crystals [4]. Recently, we have achieved drastic improvement in the energy and the memory holding time by employing InGaAsP photonic crystals [5]. Figure 3 shows our latest result of the static and dynamic bistable operation. The output signal intensity is switched between ON and OFF by applying optical set and reset pulses. The energy and power consumption for the bistability onset are 24 fJ/bit and 10 μW, respectively, which are 40 times smaller than our previous data and more than 100 times smaller than conventional optical bit memories [6]. The memory holding time is 250ns, nearly equal to 40Gbps, 12kByte-long Ethernet packet.

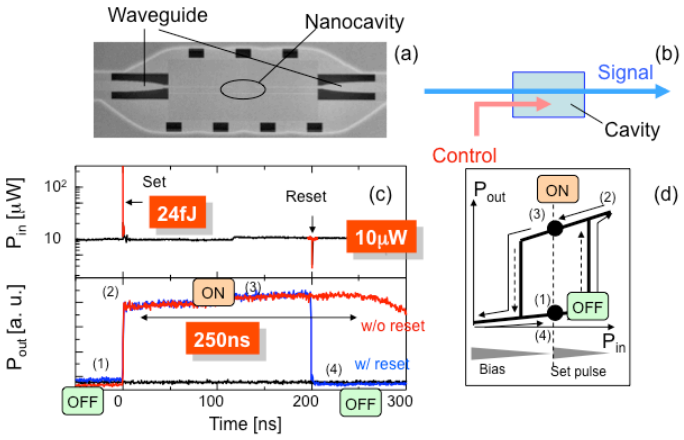

Fig.3 Photonic-crystal nanocavity-based optical bistable device: (a) Schematic view and (b) Static and dynamic bistable operation

3.2 Serial-to-parallel and parallel-to-serial converters

The all-optical serial-to-parallel bidirectional converter (SPC/PSC) in Fig.4 plays a critical role as an interface for the optical memory cells. It is based on a surface-normal all-optical switch operating with a differential spin-excitation method. The optical switch exhibits extremely high on/off ratios of over 40 dB and an ultrafast rectangular-

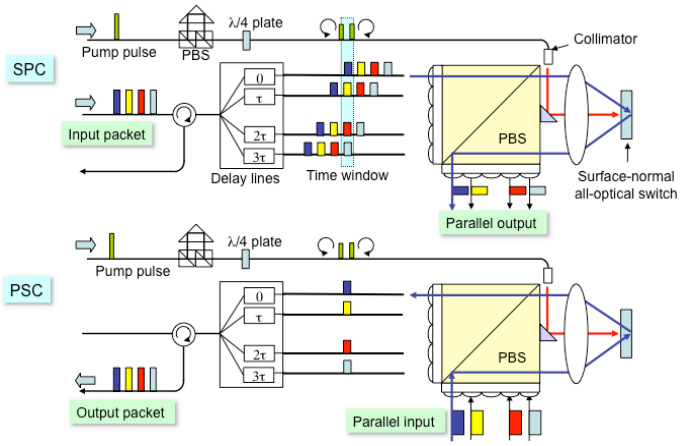

Fig.4 All-optical serial-to-parallel and parallel-to-serial converters

like switching window of which duration can be optimized for the signal bit-rate after fabrication (60 ps to 300 fs). 1:16 SPC modules have so far been demonstrated for 40-Gbit/s, 100-Gbit/s, and 1-Tbit/s burst-mode optical packets [7]. In this project, the compact SP/PS bidirectional converter were developed together with a burst-mode optical clock generator for driving the converter.

3.3 Optical beam addressing system

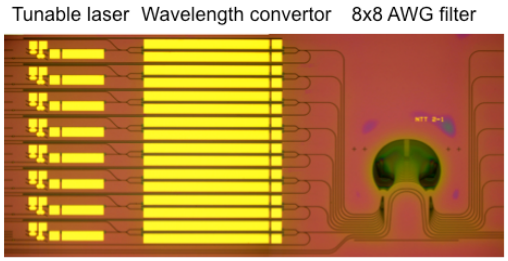

Fig.5 (a) Waveguiding optical addressing using wavelength converter and AWG

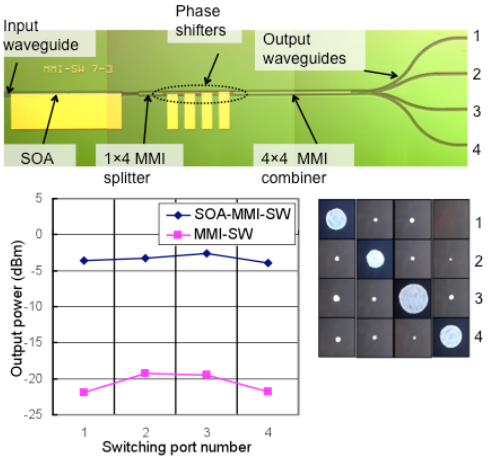

Fig.5 (b) Spatial optical addressing using MMI waveguide switch

There are two alternatives for addressing optical beam to a desired optical bit memory; one is based upon wavelength routing scheme, and the other is space optics. These devices will be placed in front of the serial-to-parallel converter and act as the optical beam addressor, which guides input packet to a designated array of optical bit memories through the serial-to-parallel converter. The monolithically integrated device consisting of a wavelength converter, a wavelength tunable laser, and an arrayed waveguide grating (AWG) filter is shown in Fig. 5(a). We used double-ring-resonator-connected tunable laser which has simple and small structure and is suitable for integrating the waveguide structure filter such as AWG filter. Fig.5(b) shows the insertion loss-free 1×4 InGaAsP/InP multimode interference waveguide switch integrated with optical amplifier [8]. The crosstalk and extinction ratio are -11.6 dB and 11.9 dB, respectively. By comparing the present SOA-MMI-SW and MMI-SW without an SOA, the output powers from each port in switching are -4 dBm and -20 dBm, respectively. The value of the loss compensation is more than 12 dB and ensures lossless optical beam addressing.

4. Conclusion

The five-year-long project to investigate an all-optical RAM buffer subsystem has been described. To sum up the achievements, the nanocavity-based optical bit memory has the onset energy of 24 fJ/bit, memory holding time of 250ns, and memory access time up to 10 GHz which is ten times faster than conventional electronic RAM. Furthermore, novel high-speed optical interfaces such as beam addressing optics and optical serial-to-parallel / parallel-to-serial converters enable us to construct an all-optical RAM subsystem that can handle burst-mode ultrafast optical packets beyond 100G. If this all-optical RAM buffer is adopted, the power consumption of optical packet routers is expected to be reduced by a factor of one eighth compared to the current electronic routers. Finally, the 40-Gbit/s write-in and read-out operation of this prototype RAM buffer demonstrator will be presented on site.

Acknowledgment

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