Over-Sampling based Burst-mode CDR Technology for High-speed TDM-PON Systems

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Abstract: We review recent progress of a over-sampling based burst-mode CDR as the key PMD device for supporting next-generation, 10Gbps capable TDM-PON systems. For the essence of circuit design, its burst-mode sync time and pulse-width distortion tolerance are also presented.
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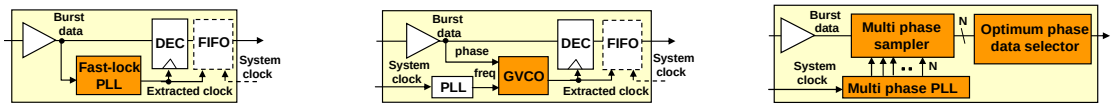
1. Introduction

The number of FTTH (Fiber-To-The-Home) users has been expanding more than 17 million as of 2009 in Japan market [1]. 10G-EPON (10-Gigabit Ethernet Passive Optical Networks) systems, which is new flavor of TDM (Time Division Multiplexing) based PON technology, holds great promise for next-generation optical access networks (NGA) because of its inherent cost-effective user-shared configuration. Followed by completion of 10G-EPON standardization in September 2009 under IEEE802.3av [2], related research activities for the 10G-EPON systems are being energetically pursued. The first 10G-EPON prototype using a XENPAK-based burst-mode optical receiver has been reported in 2005 [3]. However, the upstream throughput was limited by up to 4 Gbps due to its excessive receiver and CDR sync time of 134 usec. To break this limit, in 2007, a 10.3 Gbps burst-mode 3R receiver with a fast burst-mode sync time of 75 ns, which was composed of an gain switching TIA, an AOC (Automatic Offset Compensation) LA and a Gated-VCO based CDR (Clock and Data Recovery) chipset, was proposed in [4]. The burst-mode 3R will show the possibility of future 10 Gbps-based upstream transmissions with full throughput.

For such a high-speed burst-mode 3R circuit, CDR is especially a key element to achieve rapid burst-mode operations, because quick frequency and phase locking by poor information from short preamble bits of varied burst packets is intrinsically difficult technical issue which not handled by a normal feedback-controlled PLL based CDR. To overcome this challenge, mainly three types of burst-mode CDRs are proposed as shown in Fig.1: (a) a fast-lock PLL based CDR [5], (b) a Gated-VCO based CDR [6], and (c) a over-sampling based CDR [7-9]. The fast-lock PLL based and the Gated-VCO based CDR are clock (phase) extraction types and their sync times are controlled by adjusting the loop bandwidth (e.g. up to a few tens of MHz). However, such a wide-bandwidth loop tends to enhance the output jitter and its bursty clock extracted from incoming burst data could prevent smooth connection to upper MAC and system circuits. Thus, a very careful loop design is essential for balancing reducing jitter, elevating pulse-width distortion tolerance [10] and achieving fast sync time. On the other hand, the over-sampling based CDR can provide higher pulse-width distortion tolerable burst-mode operations with rapid sync time of within a few preamble bits [7], because it can be always operated under the stable system clock independent of fluctuations of burst packets [10]. The comparison results of sync time and pulse-width distortion tolerance are also summarized in Table1. The over-sampling CDR will be better suitable choice for PON upstream's burst-mode CDR and receivers.

In this paper, we focus on the over-sampling based burst-mode CDR and its integrated burst-mode optical receiver technology for NGA TDM-PON. Its rich characteristics for PON are reviewed and the latest performance results of 10G-EPON over-sampling based burst-mode CDR with 82.5 GS/s sampling technology are also presented.



(a) Fast-lock PLL based CDR (b) Gated-VCO based CDR (c) Over-sampling based CDR

Figure1. Configurations of burst-mode CDR for high-speed TDM-PON systems

Table1. Comparison results of burst-mode sync time and pulse-width distortion tolerance

Burst-mode CDR type	Burst-mode sync time	Pulse width distortion tolerance	Description
IEEE802.3av	400 ns	+/- 0.53 UI[*1]	*1 Defined as Dj
Fast PLL based CDR	100 ns[*2]	+/- 0.22 UI[*2]	*2 Optical input [5]
GVCO based CDR	25 ns[*3]	+ 0.22 / - 0.32 UI[*3]	*3 Electrical input [6]
Over-sampling based CDR	6.4 ns[*4]	+/- 0.53 UI[*5]	*4 Electrical input [9] *5 Optical input, BER=10^{-3} [8]

2. Concept of over-sampling based burst-mode CDR

Figure 2 shows the concept of the over-sampling based burst-mode CDR method. The basic flow of the over-sampling based CDR functions is: (i) counting data (falling/rising) edge phases with pre-designed bit intervals, (ii) judging the most reliable edge phase by majority decision from rising and falling edge phases counting distributions (e.g. phase #0 in Fig.2.), (iii) decide the optimum recovery phase which has largest phase margin from the judged edge phase result (e.g. phase #2 in Fig.2.), (iv) selecting the data which sampled by the decided recovery phase clock as the optimum CDR recovery data. The important point of the over-sampling based CDR technique is that the incoming burst data can be sampled by the multiple phase clocks synchronized with the stable system clock and the burst data can be rapidly converted to the recovery data synchronized with the upper system. Therefore, the over-sampling method is essentially appropriate for a instantaneous burst-mode CDR associated with the system circuits. The burst-mode sync time is determined by the edge phase counting bit interval (e.g. 64 bits). In principle, the first-bit data recovery can also be possible under optimum bit interval time setting condition [9]. In addition, the over-sampling CDR enables to provide precise decision-logic of the optimum recovery phase by the high accuracy major phase extraction based on a pulse-width detection technique under the very short counting time [10]. This optimum recovery phase decided function is in contrast with the long decision-time of the PLL based loop.

For another attractive feature, the over-sampling based CDR can provide dual-rate operation in the same platform. Figure 3 shows the schematic of the 10.3-Gbps/1.25-Gbps dual-rate optimum recovery data decision-logic for 10G-EPON systems [9]. In the dual-rate logic, when a 10.3 GHz x 8 phase sampling CDR receives 10.3 Gbps data, the judged optimum recovery phase is almost constant and directly outputted as recovery data. On the other hand, in case that the sampling CDR receives 1.25 Gbps data, the 1.25 Gbps data is handled with 10.0 Gbps data (1.25 Gbps x 8). When the sampling CDR samples it by the 10.3 GHz clocks, the optimum recovery phase moves little by little due to reference frequency difference between 10.3 GHz and 10.0 GHz. This causes the redundancy sampling of one bit of the 10.0 Gbps data at 33 cycles x 10.3 GHz clocks from relationship of 10.3 GHz : 10.0 GHz = 33 : 32. 10 Gbps data can be recovered by deleing this redundancy bit, e.g. of b3 in Fig.3, at every 33 x 10.3 GHz clock cycle. Finally, the recovered 10 Gbps data is converted to the complete 1.25 Gbps data by 1/8 bit skipping.

Figure 4 (a) shows the block diagram of a 82.5 GS/s (10.3 GHz x 8 phase) sampling burst-mode CDR [7] based on the over-sampling concept. The sampling circuit integrates two blocks: a 10.3 GHz x 8 phase PLL and a 82.5 GS/s sampler circuit. These 10.3 GHz clocks are synchronized with the system clock at 161 MHz. The sampler circuit can sample the incoming burst data at over 82.5 GS/s equivalent rate via the 10.3 GHz x 8 phase-shifted clocks. These high-speed sampling circuits was fabricated in IC by 0.13 um SiGe BiCMOS with ft = 200 GHz as shown in Fig.4 (b). A dual-rate data selector logic circuit including a dual-rate data decision-logic circuit and a rate correct circuit was realized in FPGA.

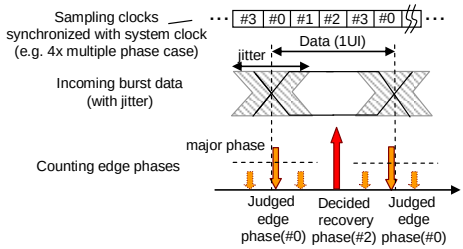


Figure2. Concept of the over-sampling CDR method

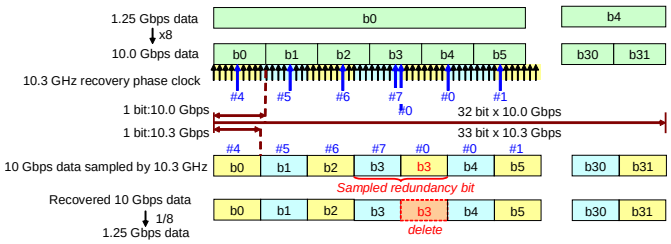


Figure3. Dual-rate recovery data decision- logic of the over-sampling CDR

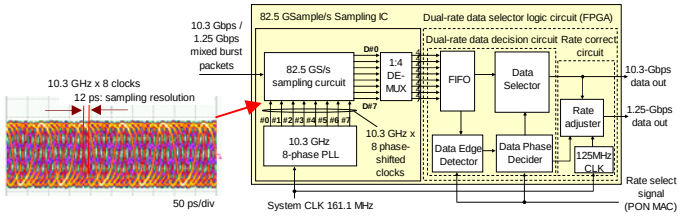


Figure4 (a). Block diagram of the 82.5 GS/s sampling based burst-mode CDR

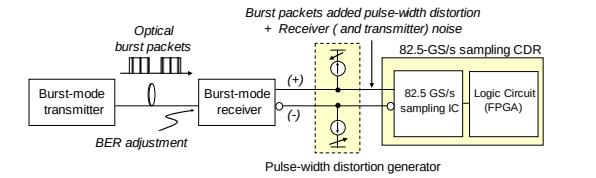
Figure4 (b).Photograph of the 82.5 GS/s sampling IC

3. Performance results

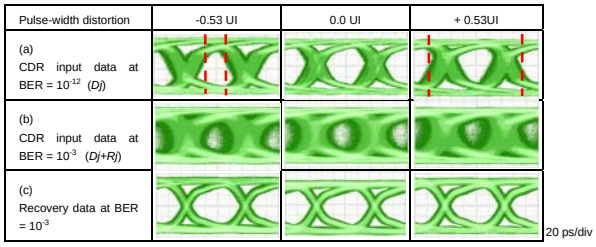
We introduce resent experimental results of the over-sampling based CDR. For the over-sampling based CDR, the pulse-width distortion tolerance as the key parameter for the burst-mode CDR design can be improved by speeding

up of the sampling resolution because the high-speed sampling can track very narrow eye-opening regions of the input burst data. Figure 5 (a) shows the experimental setup of the burst-mode pulse-width distortion tolerance test for the 82.5 GS/s sampling CDR. In the test, a 1.27 um burst-mode transmitter [11] and a burst-mode optical receiver (Rx) consisted of a APD-TIA and a LA with continuous gain and threshold varied burst-mode AGC/ATC functions [12] were employed and attached to the CDR input. A pulse-width distortion generator was inserted to add any pulse-width distortion onto the optical receiver output without degradation of the received sensitivity. Figure 5 (b) shows the measured eye waveforms of CDR inputs and recovered data. The added pulse-width distortion of +/- 0.53 UI is corresponded to the worst *Dj* (deterministic jitter) of the 10G-EPON system jitter requirement. As shown in the Fig.5 (b), it is found that the sampling CDR can recover clear data from distorted input data added +/- 0.53 UI pulse-width distortion plus large receiver output jitter of BER = 10^{-3} as RS(255,223) FEC input BER. Burst-mode BER performance without penalty at BER = 10^{-3} under +/- 0.53 UI added conditions have been also reported in [8].

Figure 6 shows experimental results of the burst-mode sync time of the 82.5 GS/s sampling CDR with the Rx at both for 10.3-Gbps and 1.25-Gbps operating mode. In the test, it was measured that a worst convergence time of CDR decision phase transient changes when 1st optical packet of phase = 0-degree was quickly alternated with no guard time to the neighboring 2nd packet of inverse phase = -180-degree at 10G-EPON required BER conditions adjusted by the Rx input optical powers. The input optical powers of 1st and 2nd packets were set to the same power in order to take no account of the Rx's burst-mode response. The edge phase counting bit intervals were set to 64 bit at 10.3 Gbps mode and 16 bit at 1.25 Gbps mode respectively. Transient waveforms of the Rx inputs and the CDR outputs are also shown as inset in Fig.6. At 10.3-Gbps mode, as shown in Fig.6 (a), it can be found that the sampling CDR can quickly follow the received data phase inverse-changes within 37 ns at BER = 10^{-3}. In addition, measured results of the sync time and transient waveforms at 1.25-Gbps mode are shown in Fig.6 (b). At input BER = 10^{-12} as no FEC condition, a fast sync time of less than 64 ns at 1.25-Gbps mode was also successfully observed. These obtained sync times are far superior to the standard value of 400 ns specified at both bit-rates mode, due to the fairly accurate and rapid burst-mode operations of the over-sampling based burst-mode CDR technique.

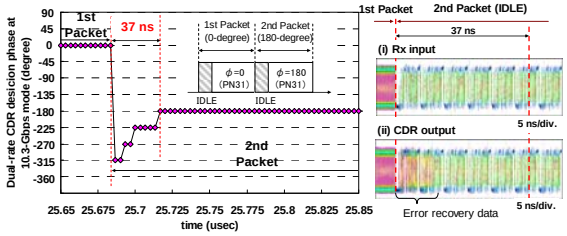


(a) Experimental Setup

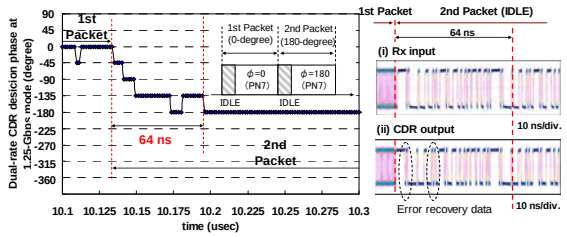


(b) Measured eye-waveforms

Figure5. Burst-mode pulse-width distortion tolerance test results



(a) 10.3-Gbps mode, BER = 10^{-3}



(b) 1.25-Gbps mode, BER = 10^{-12}

Figure6. Burst-mode sync time test results

4. Conclusions

In this paper, we have reported recent progress and performance results of the over-sampling based burst-mode CDR. As the key technology for enabling next-generation high-speed optical access systems providing over 10 Gbps per user bandwidth, the over-sampling based bust-mode CDR and its integrated burst-mode optical receivers will strongly support wide spreading of the high-speed NGA TDM-PON systems.

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