FPGA Verification of a Single QC-LDPC Code for 100 Gb/s Optical Systems without Error Floor down to BER of 10^{-15}

Deyuan Chang[1], Fan Yu[1], Zhiyu Xiao[1], Yang Li[1], Nebojsa Stojanovic[2], Changsong Xie[2], Xiaozhong Shi[1], Xiaogeng Xu[1], Qianjin Xiong[1]

[1]Huawei Technologies Co., Ltd., Network Research Department, Shenzhen, 518129, China
[2]Huawei Technologies Duesseldorf GmbH, European Research Center, Riesstrasse 25, D-80992 Munich, Germany
ader@huawei.com

Abstract: We present FPGA-based emulation results of a single QC-LDPC code with 20% redundancy designed for applications in 100 Gb/s optical transmission systems. Error floor-free transmission can be achieved at BER of 10^{-15} with a Q factor of 5.9 dB.
OCIS codes: (060.2330) Fiber optics communications; (060.4510) Optical communications

1. Introduction

Advanced forward error correction (FEC) codes are desirable for increasing transmission distance of coherent optical transmission systems. A digital coherent receiver with polarization-division-multiplexed quadrature phase-shift keying (PDM-QPSK) modulation has almost become a standard in 100 Gb/s long-haul transmission system [1-3]. Besides enabling enhanced digital signal processing algorithms, high-speed analogue-to-digital converters (ADCs) also facilitate the use of soft-decision FEC (SD-FEC) in digital coherent receivers. Paid by larger complexity, SD-FEC codes result in higher net coding gain (NCG) compared to hard decision FEC (HD-FEC) codes. Thanks to fast IC technology development, the implementation of complex SD-FEC codes for 100 Gb/s transmission system is becoming the reality [4].

Based on investigations in the past decade, quasi-cyclic low-density parity-check (QC-LDPC) codes seem to be most promising candidates for SD-FEC codes in high-speed optical systems. Designed carefully, QC-LDPC codes provide excellent error correction performance. Additionally, QC-LDPC coding schemes enable efficient parallelization resulting in relatively low circuit complexity.

In optical communication systems, there is a very strong demand on the required error-free transmission with a bit error rate (BER) less than 10^{-15}. Since all turbo decoding schemes suffer from the error floor, QC-LDPC codes are also prone to this effect. One approach to suppress or completely eliminate the error floor is the concatenation of QC-LDPC with other codes. Concatenation of the QC-LDPC and Reed-Solomon (RS) codes was proposed in [5]. The LDPC code alone without the RS code experiences the error floor at BER of 10^{-9}. The outer code suppresses the error floor and achieves BER of 10^{-13} at a Q = 7.1 dB. A better performance of the concatenated LDPC code is reported in [6]. With the same redundancy of 20.5 % as in [5], the Q factor was improved by about 1.3 dB (proved by FPGA emulation).

The concatenation of codes brings additional drawbacks. According to the FEC overhead (OH) limit of 20%, which is suggested by the OIF in [7], the concatenation reduces the overhead of the QC-LDPC inner code that limits the maximum achievable NCG. Next, the complexity may become significant since the concatenation scheme requires an outer code and an additional interleaver (deinterleaver) to decorrelate the data sequences between the component codes. Finally, more latency may come from the outer code. Thus, there is a higher motivation to find a single LDPC code with low error floor like in [8] than to focus on concatenated codes.

In this paper, we propose a single QC-LDPC code with 20% OH. To the best of our knowledge, this is the first report about FPGA-based verification of soft-LDPC codes proving transmission without error-floor down to BER of 10^{-15}.

2. QC-LDPC Code Construction and Algorithms for Soft Decision Decoding

We put following requirements on the LDPC code design: minimum NCG of 11 dB, FEC OH of 20 %, low implementation complexity and the error floor below BER of 10^{-15}. Honestly, the last requirement took us the most time during the code development. Although irregular LDPC codes can achieve better BER performance than regular LDPC codes, we did not investigate such codes since they suffer from higher error floor than regular LDPC codes [9].

The error floor strongly depends on the column weight of a parity check matrix as increasing the column weight corresponds directly to suppressing the error floor [10]. On the other hand, the computational complexity of LDPC decoding is proportional to the column weight. Influenced by the performance-complexity trade-off, the column weight of 4 was selected.

Girth and codeword length of an LDPC code also influence the error floor level. Of course, larger girths are preferred. Since we wanted to keep the code redundancy below 20%, we tried to find LDPC codes of girth 10 with minimum possible code length. The probability to find large girth LDPC codes is proportional to the codeword length. According to the rough estimation presented in [5], a girth of 10 can be obtained with codeword lengths of roughly 20000. Such long codes result in more complex ASIC design and require sophisticated optimization to reduce the implementation complexity as described below. Some results of LDPC codes with large girths are reported in [11]. So far, no any LDPC code with 20 % redundancy and a girth of 10 was reported with a verified error-floor below BER of 10^{-15}.

As illustrated in Fig. 1, the proposed single QC-LDPC FEC for 100 Gb/s transport system is supposed to be embedded in an ASIC chip together with equalization and synchronization circuits. At the transmitter side, input information is encoded using the QC-LDPC encoder and passed to the PDM-QPSK modulator. At the receiver side, the coherently detected signal is sampled by four ADCs that are integral parts of the ASIC block. The quantized signal is processed in an equalizer that outputs *n*-bit samples later used in the soft LDPC decoder.

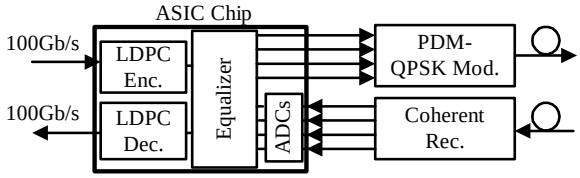

Fig. 1. Coherent transceiver including soft FEC

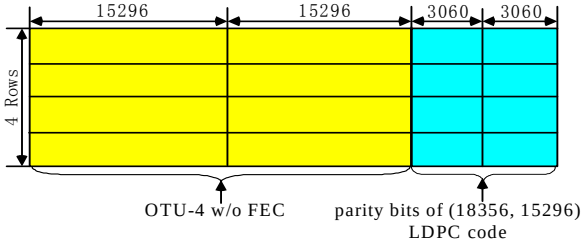

Fig. 2. FEC OTU-4 framing

The parity check matrix of QC-LDPC codes consists of an array of sub-matrices as follows:

$$H_{qc} = \begin{pmatrix} A_{1,1} & A_{1,2} & \cdots & A_{1,n} \\ A_{2,1} & A_{2,2} & \cdots & A_{2,n} \\ \cdots & \cdots & A_{i,j} & \cdots \\ A_{m,1} & A_{m,2} & \cdots & A_{m,n} \end{pmatrix}, \quad (1)$$

where each sub-matrix $\boldsymbol{A}_{i,j}$ is a $p \times p$ circulant matrix over GF(2). To facilitate the implementation of the layered decoding algorithm, the column weight of all sub-matrixes was set to 1 (so-called permutation matrix). We use $A_{i,j}^{\alpha(i,j)}$ to denote the (i, j)-th sub-matrix, whose first row has only one non-zero entry equal to 1 at the $\alpha(i, j)$-th position. Such QC-LDPC codes have a codeword length of $p \cdot n$ and an OH of $m/(n - m)$.

Since we already selected the column weight $m = 4$, we found that the row weight of 24 fulfills the OH requirement. Due to OTU-4 framing restrictions, the parameter $p = 765$ was selected. We searched for QC-LDPC codes of girth larger than 6 by using the progressive edge growth (PEG) algorithm to choose each $\alpha(i, j)$. A QC-LDPC code (18360, 15300) has been found with a girth of 8. The code was shortened due to OTU-4 framing, which is illustrated in Fig. 2 (two codewords per row).

The implementation of LDPC codes with a long codeword (e.g. 20000) is not straightforward. Fortunately, there are many optimization techniques simplifying this task. We used a modified "offset min-sum" decoding algorithm with multi-thresholds for adjusting the offset factor. This way, the circuit complexity was decreased without sacrificing error correction capability. The layered decoding algorithm was also modified by dividing each layer into sub-layers to enable the pipeline architecture. In the layered decoding algorithm, the number of quantization bits was set to 4 to additionally simplify the implementation. Using simplification techniques, the implementation complexity of our QC-LDPC (18356, 15296) code was reduced down to 50 %. Hopefully, further realization simplifications will be found in the near future so that longer and more efficient LDPC codes can be used in high-speed optical systems.

3. Emulation results

To reach a post-FEC BER down to 10^{-15}, the FPGA emulator system was built of three FPGA boards, with two Altera GX530 devices on each FPGA board (Fig. 3). Flexible to extend the emulator system, each FPGA device is an independent FEC emulation platform that includes a random codeword generator, an AWGN generator, and a QC-LDPC decoder. The design of the AWGN generator in each FPGA device was based on the quantized version of the Box-Muller method. It generates a random sample with Gaussian distribution using two uniformly distributed

random samples. Instead of the traditional linear feedback shift register (LFSR), the Tausworthe uniform random number generator with a sufficiently long period is used in each AWGN generator with different seeds. Since we used the layered min-sum algorithm with 4 soft-decision bits, the throughput of the FPGA emulator system reached nearly 10Gb/s.

Fig. 4 shows FPGA emulated BER performance of the described code. The maximum number of iterations is set to 6, 9, and 12 (including initialization). Consistent with the computer simulation (CS), FPGA emulation results with 6 and 12 iterations differ by only 0.2dB, which proves very fast convergence of the layered decoding process. The LDPC code experiences the error floor slightly above 10^{-15}, which was suppressed below 10^{-15} using a simple post-processing method (PPM) of negligible complexity [12]. Such a low error floor of the girth-8 LDPC code may be due to the good trapping set spectrum of the code [13], which is still under our investigation. When the number of iterations (I_{max}) is set to 12, the code achieves a Q-limit of 5.9dB at a post-FEC BER of 10^{-15} that corresponds to an NCG of 11.3dB.

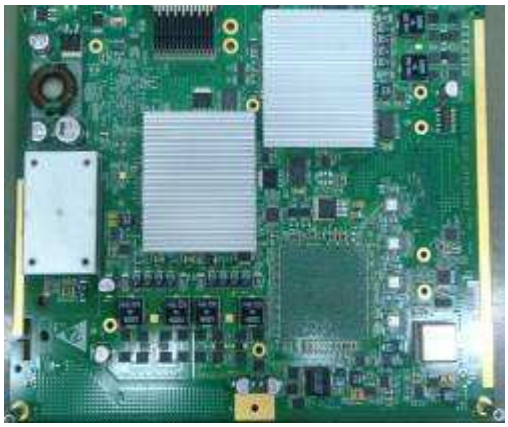

Fig. 3. One FPGA board of the emulator system

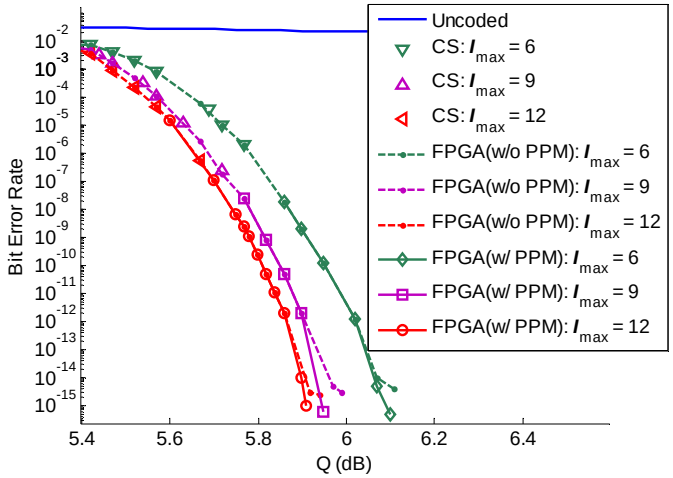

Fig. 4. Emulation results

4. Conclusion

We proposed a non-concatenated girth-8 QC-LDPC code with 20% OH for 100 Gb/s optical transmission systems. The code performance was verified by the use of an FPGA emulator system. Superior performance is demonstrated at a post-FEC BER of 10^{-15}: no error floor, a Q-limit of 5.9dB, and an NCG of up to 11.3dB. Thanks to optimization techniques, the implementation complexity of the proposed coding scheme is reduced by half. We believe that the proposed non-concatenated QC-LDPC code is a promising solution for 100 Gb/s systems.

References

[1] C. S. R. Fludger, *et al*., "Coherent equalization and POLMUX-RZ-DQPSK for robust 100-GE transmission," *IEEE J. of Lightwave Technol.*, vol. 26, no. 1, pp. 64-72, 2008.

[2] J. Renaudier, *et al*., "Transmission of 100Gb/s coherent PDM-QPSK over 16x100km of standard fiber with allerbium amplifiers," *Opt. Express*, vol. 17, no. 7, pp. 5112-5119, 2009.

[3] J. X. Cai, *et al*., "Transmission of 96x100G pre-filtered PDM-RZ-QPSK channels with 300% spectral efficiency over 10,608km and 400% spectral efficiency over 4,368km," *OFC2010*, PDPB10.

[4] S. S. Iyer and E. J. Nowak, "45nm SOI and beyond – getting to a general purpose technology," *IEEE International SOI Conference*, Indian Wells, CA, pp.1-4, 2007.

[5] Y. Miyata, *et al*., "Efficient FEC for optical communications using concatenated codes to combat error-floor," *OFC2008*, OTuE4.

[6] N. Kamiya, *et al*., "Concatenated QC-LDPC and SPC codes for 100Gbps ultra long-haul optical transmission systems," *OFC2010*, OThL2.

[7] Optical Internetworking Forum (OIF), "*100G Forward Error Correction White Paper*," http://www.oiforum.com.

[8] T Mohsenin, *et al*., "Trends and Challenges in LDPC hardware decoders," *IEEE Asilomar Conf. on Sig., Sys. & Computers (ACSSC)*, Pacific Grove, CA, pp. 1273-1277, 2009.

[9] S. Gounai, *et al*., "Lowering error floors of irregular LDPC code on fast fading environment with and without perfect CSI," *IEEE Vehicular Technology Conference 2005*, Stockholm, Sweden, pp. 634-638, 2005.

[10] H. Zhong, *et al*., "Quasi-Cyclic LDPC Codes for the Magnetic Recording Channel: Code Design and VLSI Implementation," *IEEE Trans. Magnetics*, vol. 43, no. 3, pp. 1118-1123, 2007.

[11] I. B. Djordjevic, *et al*., "Large girth low-density parity-check codes for long-haul high speed optical communications," *OFC2008*, JWA53.

[12] Z. Zhang, *et al*., "Lowering LDPC error floors by postprocessing," *IEEE Global Comm. Conf. (GLOBECOM)*, New Orleans, LA, Nov. 2008.

[13] L. Dolecek, *et al*., "Towards improved LDPC code designs using absorbing set spectrum properties," *IEEE Int. Symp. on Turbo Codes (ISTC)*, Brest, France, Nov. 2010.