

# Monolithically Integrated Compact VMUX/DEMUX on Silicon-on-Insulator Platform

Dazeng Feng, Ning-Ning Feng, Cheng-Chih Kung, Hong Liang, Wei Qian,  
Joan Fong, B. Jonathan Luff and Mehdi Asghari

Kotura Inc., 2630 Corporate Place, Monterey Park, CA 91754, USA  
[dfeng@kotura.com](mailto:dfeng@kotura.com)

**Abstract:** We demonstrate a compact 40-channel, dense wavelength division multiplexing (DWDM) VMUX/DEMUX by monolithic integration of an echelle grating and high-speed p-i-n VOA on the silicon-on-insulator (SOI) platform. The demonstrated device has low optical loss, low PDL, fast attenuation response speed and an area of only 25mm by 10mm.

©2011 Optical Society of America

OCIS codes: (130.7408) Wavelength filtering devices, (130.3120) Integrated optics devices, (250.5300) Photonic integrated circuits.

## 1. Introduction

The use of reconfigurable optical add/drop multiplexing (ROADM) systems is rapidly expanding, because this approach offers a high level of flexibility and intelligence to the optical network. A compact and single chip variable optical attenuator (VOA) array integrated with multiplexer/demultiplexer (VMUX/DEMUX) devices forms one of the key components in a ROADM system. To date, several single chip or multichip based VMUXes have been demonstrated, these are mainly based on the silica planar light circuit (PLC) platform [1-2]. Silica PLC based VMUX solutions usually suffer from a large chip size, high power consumption and high polarization dependent loss (PDL) at high attenuation levels. The silicon-on-insulator (SOI) platform has the best and most understood material system, is compatible with mature silicon IC manufacturing processes, provides a broad range of functionalities and so offers a very attractive alternative approach to the development of low cost photonic components like the VMUX/DEMUX [3-7]. In this paper, we demonstrate for the first time, a compact, low loss and high speed monolithically integrated VMUX/DEMUX on the SOI platform by monolithic integration of 40 VOAs with a 40 channel flat-top echelle grating based on the 100G ITUT grid. The high performance echelle grating performs the multiplexing/demultiplexing function and the solid state p-i-n current injection based VOA provides high-speed optical power adjustment for each channel. We have chosen to use an echelle grating because of its significant size advantage compared to the arrayed waveguide grating (AWG). A 100GHz channel spacing flat-top device with an area of 25mm x 10mm, less than 5.0dB on chip optical loss, and better than 30dB channel isolation has been demonstrated. The echelle grating has less than 0.5dB of PDL as its polarization dependant wavelength (PDW) shift is compensated. The VOA has low power consumption, almost no additional PDL and can operate at more than 3MHz attenuation speed.

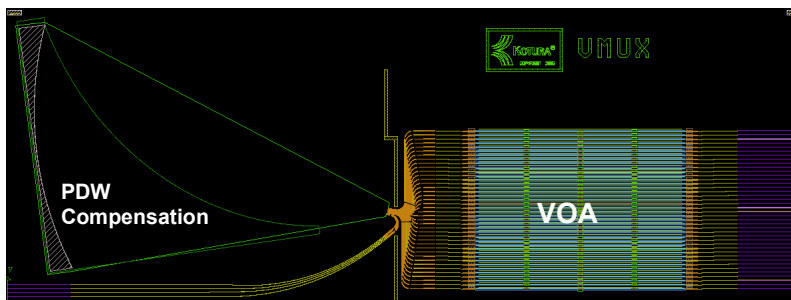


Fig. 1: Mask layout of the VMUX/DEMUX chip

## 2. Device design and fabrication

An overall mask layout of the VMUX/DEMUX device is shown in Figure 1. The device consists of a 40 channel echelle grating demultiplexer and an array of 40 channel VOAs. The echelle grating was designed with 100GHz

channel spacing and flat-top passband. In our design, a 3  $\mu\text{m}$  height silicon waveguide core size was chosen so that the device has a much better fabrication tolerance than if it was fabricated using sub-micron silicon waveguides. The flat-top passband was achieved by a 1x2 multimode interference (MMI) structure giving a double peak optical profile just before entering into the slab region of the echelle grating. The grating line was adjusted from a Rowland circle mounting to minimize astigmatism. The intrinsic PDW of a 3  $\mu\text{m}$  silicon slab is about 350 pm. This would cause large PDL for the 100GHz spacing filter, but the PDW can be reduced by shallow etching a prism-shaped region in the slab region [8]. Figure 2 (a) shows simulation results for the PDW and transition loss dependence on the etch depth of the PDW region. When the etch depth is 0.25  $\mu\text{m}$ , the PDW can be reduced to almost zero while the additional loss penalty is only about 0.1dB. Figure 2 (b) shows simulated 40 channel spectra after the PDW is compensated. The spectra for TE and TM polarized light are almost overlapped together. The integrated VOA array is based on the free-carrier absorption effect and is implemented using a p-i-n diode structure within the silicon waveguide and controlled by current injection into the device [3]. The key advantages of a p-i-n based VOA is the low power, high speed and very low PDL even at high attenuation levels.

The device was fabricated using standard CMOS compatible processes. The waveguides were etched to 1.2  $\mu\text{m}$  to form single mode waveguides. The grating facets were etched to the buried oxide layer. A 200 nm layer of high reflectivity aluminum was deposited on the grating facets. The boron and phosphorus were diffused into the regions at either side of the waveguide to form a horizontal p-i-n junction and ohmic contact areas. The doping regions are sufficiently far away from the waveguide to prevent any optical loss. A Ti/Al metal stack was deposited and patterned to form p-type and n-type metal contacts. Finally, oxide and nitride films were deposited as waveguide cladding and passivation layers. The fabricated 40 channel VMUX/DEMUX has a footprint of 25 mm by 10 mm.

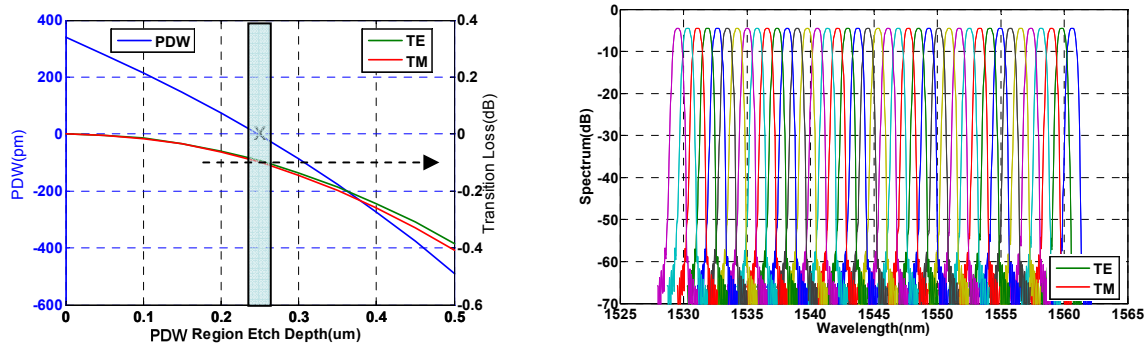


Fig. 2 (a): Simulation of PDW and transition loss vs. etching depth of the PDW region. (b): Simulated spectra after PDW compensation of both TE and TM polarizations.

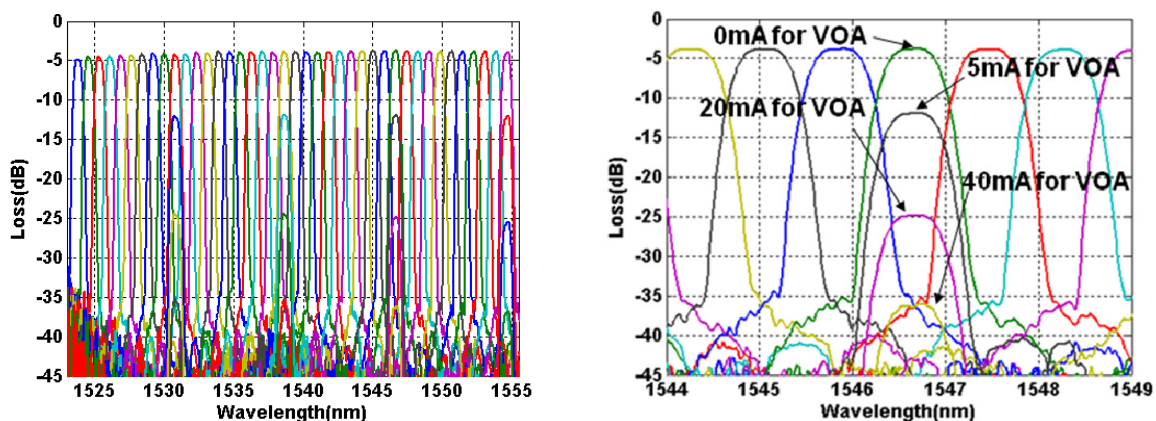


Fig. 3 (a): Measured 40 channel VMUX/DEMUX spectra. (b): Measured channel spectra after applying various currents to a VOA.

### 3. Measurement results and discussion

The fabricated device was measured using an automated measurement system. The light from a broadband amplified spontaneous emission (ASE) source was coupled to the device through a single mode fiber. The light from the

output waveguide was also coupled to a single mode fiber. The transmitted power was measured by an optical spectrum analyzer (OSA). Figure 3 (a) shows the measured 40 channel spectra of the device. The losses are normalized to a reference straight waveguide. The device has 100GHz channel spacing and a flat passband with a 1dB bandwidth of 50GHz. The on chip loss is about 5dB. The isolation between channels is better than 30dB. The PDW is below 20pm and PDL is reduced to below 0.5dB after PDW compensation is implemented. Transmissions on channels 10, 20, 30, 40 were controlled by the VOAs. Figure 3 (b) shows the detailed spectra when different currents were applied to the VOA on channel 30. The light can be attenuated by 20dB with about 20mA of current applied. Figure 4 (a) shows the VOA attenuation dependence on the applied current for all the 40 channels. Figure 4 (b) shows the measured small signal 3dB bandwidth at 5dB attenuation level. The measured 3MHz bandwidth of this device is much faster than that of MEMS and thermal effect silica VOAs.

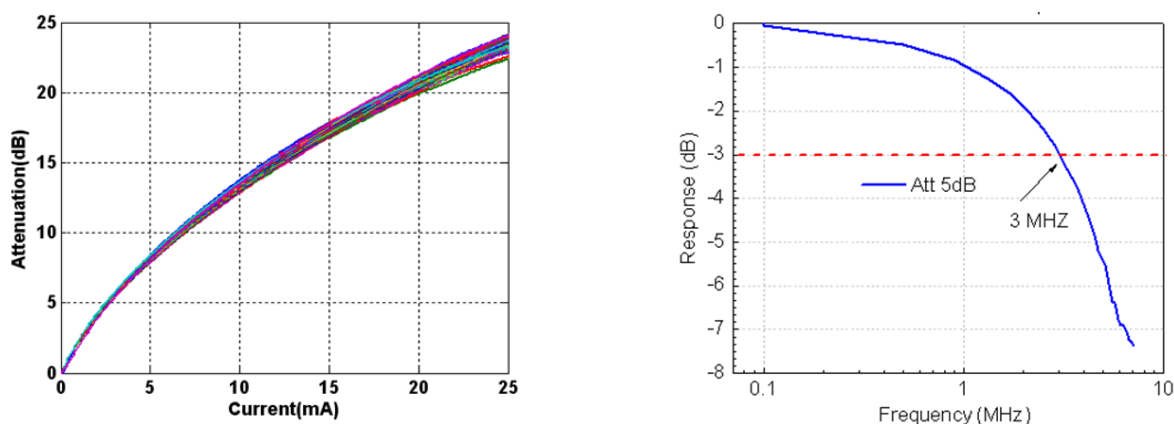


Fig. 4 (a): Measured attenuations vs. applied current for all 40 VOAs. (b): Measured frequency response for silicon p-i-n VOA.

#### 4. Conclusion

In conclusion, a 40 channel DWDM VMUX/DEMUX has been demonstrated by monolithic integration of an echelle grating and p-i-n attenuator on the SOI platform. The demonstrated device has a very compact size of 25mm x 10mm, low on chip loss of 5dB, and over 30dB channel isolation. High efficiency p-i-n current-injection based VOAs can achieve an attenuation level in excess of 20dB by application of only 20mA current and exhibit 3MHz of 3dB modulation bandwidth. The small footprints of the reported devices enable a low-cost VMUX/DEMUX solution.

#### References

- [1] I. E. Day, S. W. Roberts, R. O'Carroll, A. Knights, P. Sharp, G. F. Hopper, B. J. Luff, M. Asghari, "Single-chip variable optical attenuator and multiplexer subsystem integration." OFC 2002, Page(s): 72 – 73.
- [2] H. Nishi, T. Tsuchizawa, T. Watanabe, H. Shinojima, R. Kou, S. Park, K. Yamada and S. Itabashi, "Monolithic integration of a silica-based arrayed waveguide grating filter and silicon variable optical attenuators based on p-i-n carrier-injection structure." We.8.E.3, ECOC 2010.
- [3] Y. Nasu, K. Watanabe, M. Itoh, H. Yamazaki, S. Kamei, R. Kasahara, I. Ogawa, A. Kaneko, Y. Inoue, "Ultrasmall 100 GHz 40-Channel VMUX/DEMUX Based on Single-Chip 2.5% $\square$  PLC." J. of lightwave technology, Vol 27, 2087-2094(2009).
- [4] D. Feng, W. Qian, H. Liang, C-C. Kung, J. Fong, B. J. Luff, M. Asghari, "Novel fabrication tolerant flat-top demultiplexers based on etched diffraction gratings in SOI," 5rd Int. Conf. Group IV Photonics, P386 - 388. Sorrento, Italy (September 17-19, 2008).
- [5] B. J. Luff, D. Feng, D. C. Lee, W. Qian, H. Liang, and M. Asghari, "Hybrid Silicon Photonics for Low-Cost High-Bandwidth Link Applications," Advances in Optical Technologies, vol. 2008, Article ID 245131, 6 pages, 2008. doi:10.1155/2008/245131
- [6] N.-N. Feng, D. Feng, H. Liang, W. Qian, C.-C. Kung, J. Fong, and M. Asghari, "Low-loss polarization-insensitive Silicon-on-insulator-based WDM filter for triplexer applications," IEEE Photon. Technol. Lett., 20, 1968 (2008).
- [7] S. Bidnyk, D. Feng, A. Balakrishnan, M. Pearson, M. Gao, H. Liang, W. Qian, C.C. Kung, J. Fong, J. Yin, and M. Asghari, "silicon-on-Insulator-Based Planar Circuit for Passive Optical Network Applications," IEEE Photonics Technology Letters, vol. 18, no. 22, pp. 2392-2394, 2006.
- [8] J. -J. He, E. S. Koteles, B. Lamontagne, L. Erickson, A. Del age, and M. Davies, "Integrated Polarization Compensator for WDM waveguide demultiplexers", IEEE Photon. Technol. Lett. 11, 224-226 (1999).