Implementation of High-speed Buffer Management for Asynchronous Variable-length Optical Packet Switch

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Abstract: We develop an FPGA-based buffer management hardware with 8 input ports, which implements a parallel and pipeline mechanism to support over-200-Mpacket/s/port asynchronous variable-length optical packet switching. Optical buffering for asynchronous variable-length packets is demonstrated.

OCIS codes: (060.4250) Networks; (060.4510) Optical communications

1. Introduction

Optical packet switch (OPS) systems have been intensely investigated as node systems to provide high-throughput, energy-efficient and transparent forwarding [1]-[5]. We have also developed OPS systems for optical packets with various bit-rate and modulation format, and achieved 1.28 Tbit/s/port optical packet switching [6]-[9]. On the other hand, our OPS systems support only synchronously arriving fixed-length optical packets. To apply to synchronous fixed-length OPS systems into networks, extra loads such as packet-synchronization and adjusting packet-length are imposed on core or edge nodes. Therefore, to decrease their extra processing and realize practical networks, it is necessary for OPS systems of core nodes to directly support asynchronously arriving variable-length optical packet.

Our OPS system consists of optical switches and optical buffers in data-plane, and optical label processors and electrical buffer managers in control plane, as shown in Fig.1. Because the label processing is passively performed by an optical correlation technique [10] and control signals for optical switches are instantaneously output after processing, optical switching can be executed for asynchronous variable-length optical packets. The optical buffer consists of optical switches and optical fiber-delay-lines (FDLs) which give a fixed delay. Recently, it is reported that the buffer-size in the core node could be reduced to 10-20 packets at the expense of a small amount of bandwidth utilization [11]. However, due to the current scheduling algorithm of a buffer manager, our optical buffers only deal with synchronous fixed-length optical packets [6]-[9]. Recently, buffer management mechanisms for asynchronous variable-length optical packet have been investigated [12]-[13]. In addition, to realize higher speed processing, a parallel and pipeline mechanism on multiple processing architecture has been designed and the feasibility of implementation on field programmable gate arrays (FPGAs) for supporting 78.2 Mpacket/s/port OPS system has been confirmed by gate level simulation by assuming 0.22 μm FPGA technology in [14].

In this paper, we develop a novel buffer manager based on the parallel and pipeline mechanism of [14] for asynchronous variable-length optical buffering. The manager works for over 200 MHz, which can achieve 200 Mpacket/s/port OPS systems (it is assumed that minimum arrival interval is 5 ns (more than 100 Gbit/s at 64 byte

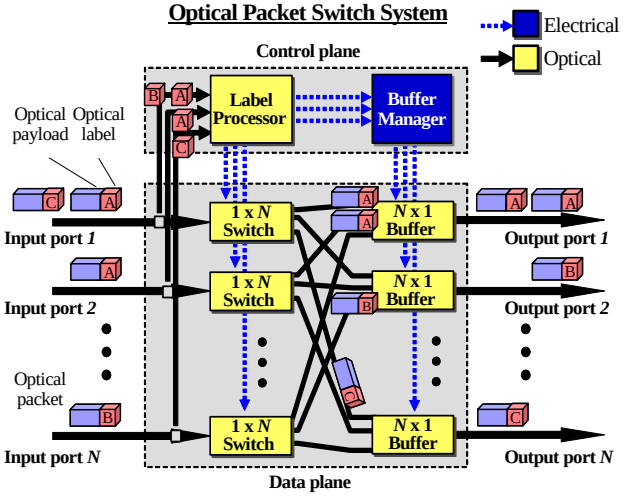

Fig. 1. Configuration of OPS system.

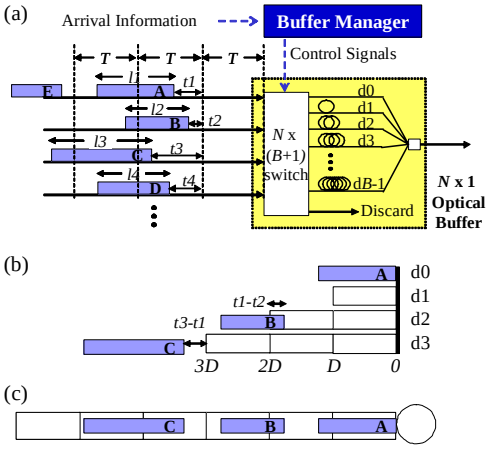

Fig. 2. (a) Configuration of optical FDL buffer. (b) Assigned FDLs and relative positions of packets (A-C) after buffering. (c) State of buffer occupancy.

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for n : = 1 to N do
begin
 if (l_n ≠ 0) then begin
  Δ_n : = ⌈(q - t_n) / D⌉
  if Δ_n < B then begin
   q : = t_n + l_n + Δ_n D;
   Packet from port n is given delay Δ_n D ;
  end
  else Packet from port n is discarded;
 end
end
q : = max(q - T, 0);
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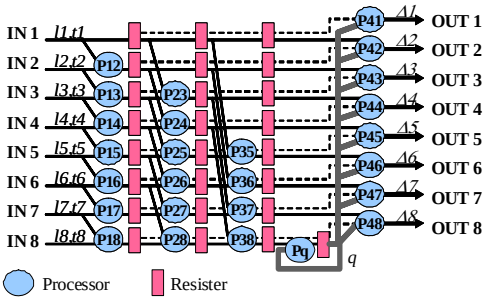
(a)



(b)

Fig. 3. (a) Pseudo-code for sequential scheduling for asynchronous variable-length optical packets from *N*-ports at a cycle. (b) Parallel and pipeline processing architecture (N = 8).

Fig. 4. Photograph of buffer manager.

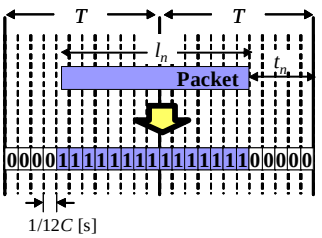
minimum packet)) by using the mechanism and a latest 65 nm FPGA technology. In this paper, we confirm the performance of the novel buffer manager and demonstrate asynchronous variable-length optical buffering on an optical FDL buffer.

2. Buffer manager based on parallel and pipeline mechanism for asynchronous variable-length OPS system

A N x 1 optical buffer consists of a N x (B + 1) optical switch, B optical FDLs with different lengths and one fiber for discard as shown in Fig.2(a). The length (d_0, d_1, …, d_{B-1}) of B FDLs are increased by the unit length D (0, D, …, (B-1)D). N is the total number of input ports. C (= 1/T) is an internal clock frequency of the buffer manager, and T represents the unit of time for sequential scheduling. The buffer manager receives the packet length l_n and the arrival gap t_n as arrival information of a packet from all input ports T seconds before optical packets arrive switches, and calculate a delay value Δ_n, which is given to each new packet coming from all ports, by using the arrival information during each cycle time T based on sequential scheduling to avoid packet collisions. Control signals for the switch corresponding to the delay value are output from the manager. Each optical packet is sent to an FDL by the switch and delayed for appropriate time. Figure 2(b) and 2(c) shows one example of assigned FDLs and relative positions of packets, and the state of buffer occupancy after buffering. The buffer manager holds variable q which represents the time at which all packets waiting in the buffer depart from the buffer. The q is used to denote buffer occupancy.

For understanding the buffer management algorithm, Fig. 3(a) shows the pseudo-code for sequential scheduling for asynchronous variable-length packets from all N-ports at a cycle, where the phrase "packet is given delay $\Delta_n D$" means that the corresponding packet is switched to delay line $d_{\Delta n}$. The above scheduling was expanded to parallel and pipeline processing for a future demand of increase in the number of ports, and the data rate because the parallel and pipeline mechanism on multiple processing architecture provides N times faster processing compared with $O(N)$ sequential scheduling, as shown in Fig. 3(b). Here, arrival information should be received 4T before packet arriving. The details of the parallel and pipeline algorithm for asynchronous variable-length packets are shown in [14].

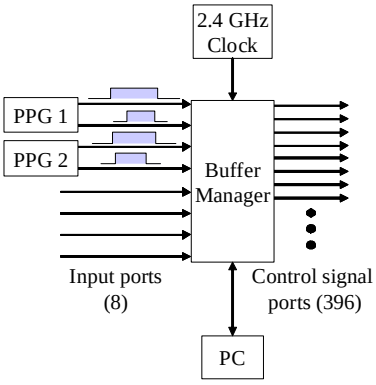
We developed a buffer management hardware with 65 nm FPGA as shown in Fig.4. The manager supports N = 8 input ports and 256 (up to 396) control signal ports for switches. The frequency C (=1/T) of an internal clock is 207.36 MHz, which generated by an external clock of frequency 2.48832 GHz. In this manager, the packet length l_n and the arrival gap t_n of a packet from port n are measured with a twelvefold frequency (= 2.48832 GHz) of the



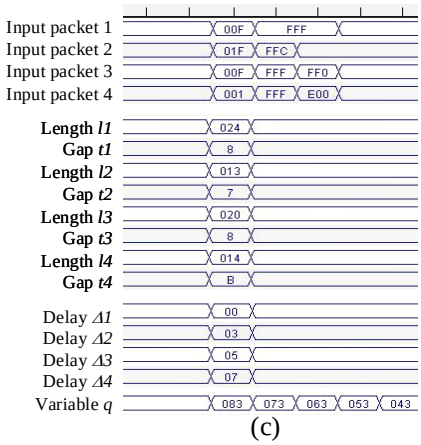
Packet length l_n : (1 + 3/12)T
→ "*13*" in Hex

Arrival Gap t_n : (5/12)T
→ "*5*" in Hex

(a)



(b)



(c)

Fig. 5. (a) Measurement of packet length and arrival gap. (b) Setup for operation confirmation of buffer manager. (c) Operation of buffer manager for asynchronous variable-length optical packets from 4 input ports.

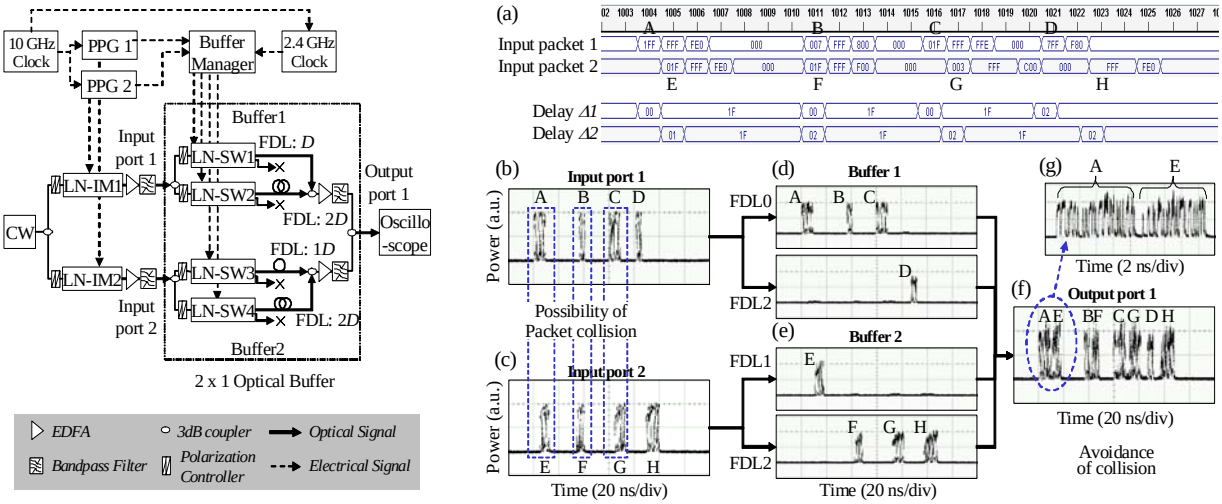


Fig. 6. Experimental setup and results of optical buffering for asynchronous variable-length optical packets from 2 input ports.

internal clock *C*, as shown in Fig.5(a). The number of packet-existing area which represents as "1" and packet-nonexistent area which represents as "0" from the starting time of a cycle are counted for measurement of the packet length and the arrival gap, respectively. Usually, their numbers are expressed in hexadecimal notation. Note that the value is rounded up if it is 12 or greater only in the last digit. To confirm of the buffer manager operation, we input electrical signals, which are used as arrival information of asynchronous variable-length optical packets, from pulse pattern generators (PPGs) into 4 input ports on experimental setup as shown in Fig.5(b). The input packets, the packet length l_n, the arrival gap t_n, the delay value Δ_n, and the variable q on FPGA are monitored at a personal computer. From Fig.5(c), it was confirmed that the length measurement of each packet from 4 input ports, and the calculation of the delay value and the variable q were correctly executed. The latency until delay calculation is 97 ns.

3. Experiment of asynchronous variable-length optical packet buffering by buffer manager

Figure 6 shows an experimental setup and results of asynchronous variable-length optical packet buffering. A signal light with wavelength of 1550.0 nm from a continuous wave (CW) laser was divided and fed into $LiNbO_3$ intensity modulator 1 and 2 (LN-IM 1, 2) to generate optical packets (A-H), whose payloads are 10 Gbit/s data-rate NRZ PN:2^9-1 and PN:2^7-1 sequences, respectively. Optical packets with different packet-length are asynchronously input into a 2 x 1 optical buffer consisting of FDLs and 1 x 2 LN switches (LN-SW 1, 2, 3, 4), which are used as gate switches to improve the extinction ratio. At the same time, electrical signals were input into a buffer manager as arrival information of optical packets. Note that we synchronized among PPGs and the buffer manager to acquire optical packet waveform by a sampling oscilloscope. Figure 6(a) shows the operation of the buffer manager at the internal clock frequency *C* of 207.36 MHz. Figures 6(b) and 6(c) show optical packet patterns in input ports 1 and 2, respectively. There are possibility of packet collisions. The buffer manager calculated the delay value and output control signals for 1 x 2 LN-SWs. The switching speed of LN-SW is below 100 ps. The unit length *D* of FDLs is 0.96 m and the maximum buffer size is 2 packets. Each packet is switched into an adequate FDL. Figures 6(d) and 6(e) show the delayed packets in buffer 1 and 2, respectively. Figure 6(f) shows merged optical packets in output port 1. Packet collisions were avoided. The doted oval shows the detail as shown in Fig. 6(g). It was confirmed that a buffer manager correctly operated for asynchronous variable-length optical packet buffering.

4. Conclusion

We developed an FPGA-based buffer manager which implements a parallel and pipeline mechanism to achieve over-200-Mpacket/s/port optical packet switching. This hardware can realize OPS systems capable of supporting asynchronous variable-length optical packets for practical networks.

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