Performance Comparison of MLSE-Based Receivers in a 1000 km Transmission Link under Fast SOP Variations

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Abstract: This paper aims at comparing the tolerance to fast SOP variations of two MLSE-based receivers. Descriptions of the emulation device and measurement method are given. The results show that the receiver architecture impacts the performance.

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1. Introduction

Since years 2000, an interest in using Maximum Likelihood Sequence Estimation (MLSE) receivers in 10 Gbps optical transmission has appeared as operators had to manage Polarization Mode Dispersion (PMD) limitations of their fibers. MLSE-based equalizers are cheaper and offer better performances than their optical counterparts [1].

MLSE tolerance to Chromatic Dispersion (CD) and/or PMD has already been extensively studied [1-3] but most of time in static configuration. However, when considering robustness to PMD, an important feature is the tolerance to State Of Polarization Variation Speed (SOP-VS). Traditionally, either worst cases SOP or low SOP-VS (less than 2°/ms) are considered when evaluating equalizers. Reference [4] compares the dynamic behavior of MLSE and FFE/DFE when facing SOP variations but no quantification in terms of SOP-VS is given. Some field measurements of SOP-VS as fast as 72°/ms are reported in reference [5] which emphasizes the fact that PMD compensators should fulfill these requirements.

In this paper, we compare the performances of two MLSE-based receivers considering SOP-VS as fast as 110°/ms in a 50 GHz-spaced 80x10 Gbps 1000 km transmission experiment. The first part of our analysis presents the experimental set-up used for the tests and the way the SOP variations are emulated and measured, while the second part details the measurement results for both receiver types.

2. Experimental set-up: 1000 km transmission link and MLSE-based receivers description

Fig. 1 shows the experimental set-up. Both positive and negative outputs of a Pulse Pattern Generator (PPG) deliver a 9.95 Gbps electrical 2^{31}-1 PRBS pattern to an FEC board. The two complementary Reed-Solomon RS (255,239) encoded signals at 10.62 Gbps feed two Lithium Niobate (LiNbO3) Mach-Zehnder modulators (Tx1, Tx2) which directly modulate in NRZ (Non Return to Zero) the 50 GHz-spaced 80 channels (going from 1532.68 nm to 1564.27 nm) coming from two interleaved combs of 40 wavelengths. The outputs of the two Tx are combined via a 50/50 coupler, and launched into the 10 spans of the transmission link, each composed of a dual-stage Erbium Doped Fiber Amplifier (EDFA), a Variable Optical Attenuator (VOA) and 100 km ITU-T G.652 fiber. An EDFA is also located at the end of the link and its output connected to a 0.28 nm (at -3 dB, 0.74 nm at -20 dB) band-pass filter which selects the measured channel feeding the receiver. A Dynamic Gain Equalizer (DGE) is inserted in the middle of the link (after 500 km transmission) in order to flatten the channel spectrum at the transmission end. The inter-stages of the 11 EDFAs house a VOA and a Dispersion Compensating Module (DCM), leading to a total residual CD around +280 ps/nm at 1560.6 nm (on the receiver). Note that a pre-compensation of -1064 ps/nm at 1560.6 nm is set in the 1st EDFA inter-stage.

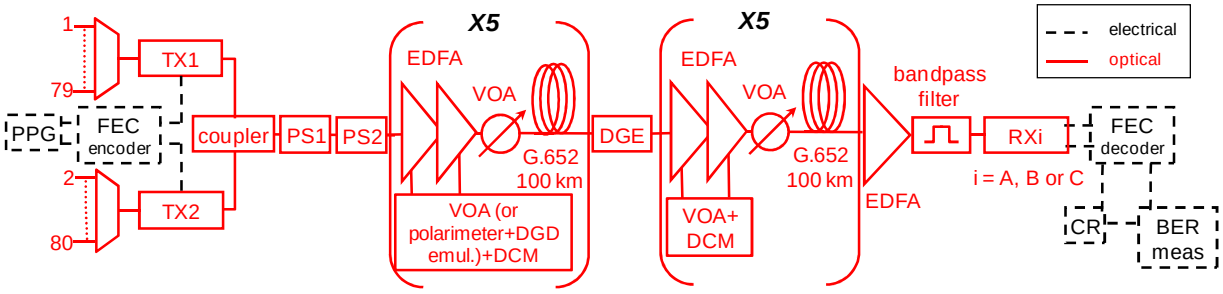

Fig. 1. Experimental set-up

With less than -1 dBm and -3 dBm per channel at the input of the G.652 fibers and the DCMs respectively, neither Self Phase Modulation (SPM) nor Cross Phase Modulation (XPM) are excited in the link. Moreover, the

regular compensation of CD along the link and low residual CD on the receiver results in a negligible CD penalty. Only the emulated PMD impacts the system performance. The emulation of first-order PMD is generated by a PE3 JDS emulator put inside the 4th EDFA inter-stage and limited to 120 ps DGD (Differential Group Delay). Polarization scrambling is performed using two scramblers (see §3) which are located before the 1st EDFA of the link.

Fig. 2 describes the three receivers under test. The 1st one (called A), acting as reference, is composed of a commercial APD with differential outputs connected to a Clock and Data Recovery (CDR) with an adaptive decision threshold. The 2nd one (B) is a commercial 16-state MLSE transponder whose optical output is connected to the APD. The 3rd one (C) is constituted of the APD followed by a commercial equalizer associating a 16-tap FFE and an 8-state MLSE. The output of the receivers (RxA, RxB or RxC) is connected (Fig. 1) to the FEC board (for FEC decoding) whose complementary outputs feed respectively the clock recovery and BER measurement test-set.

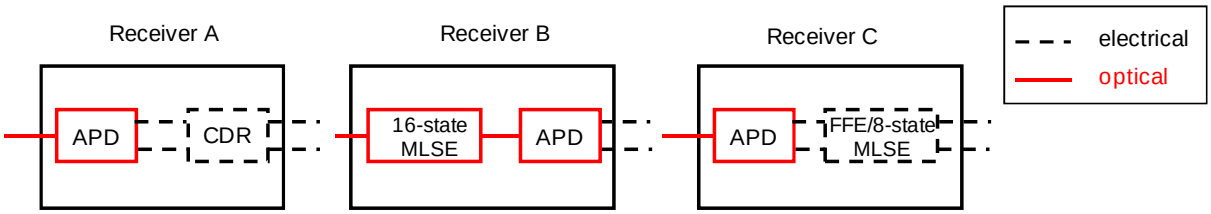

Fig. 2. Configuration of the three receivers (RxA, RxB, RxC)

3. SOP variation emulation and measurement

Two polarization controllers/scramblers are associated to create SOP variations. The 1st one is the Agilent 11896A (PS1), with 8 Scan Rate (SR) values (~ 0.03 to 1.3°/ms average SOP-VS), followed by the ex-Adaptif A2000 (PS2) used in continuous scrambling mode where the SR can take values from 1 to 1000 (~ 0.07 to 70°/ms average SOP-VS). An ex-Adaptif A1000 polarimeter with a maximum sampling rate of 1041 kHz is placed in front of the DGD emulator. Repetitive measurements of SOP variations using only PS2 show a deterministic plot on the Poincare sphere, while adding PS1 in front of PS2 produces random SOP variations at the input of the DGD emulator.

For each combination of SR (generated by the PS1+ PS2 association), the SOP-VS is measured with the A1000 polarimeter by collecting 3072 samples of Stokes parameters (S0, S1, S2, S3). The influence of the sampling time interval on maximum value of the SOP change is measured: a Rayleigh distribution of the SOP change is observed as in references [6, 7]. Experimentally, the sampling rate is carefully chosen in order to measure ~ 0.5° SOP change, while artificial variations due to over-sampling are ignored. For example, we have found that 140 kHz is a good trade-off when using PS1 (SR8) with PS2 (SR1000). Finally, we determine the SOP-VS by calculating the angle between 2 consecutive samples using the scalar product method [7].

4. Experimental results

The following results are presented at 1560.6 nm corresponding to Tx1 (odd channels) but the same results are obtained with the Tx2 channels. Fig. 3 shows the evolution of the required OSNR versus DGD at 10^{-4} pre-FEC BER and 10^{-12} post-FEC BER. The curves of Fig. 3 are deduced from the BER versus OSNR measurements obtained for various DGD with FEC "off" (pre-FEC) and FEC "on" (post-FEC). Each BER is recorded during 2 minutes. All the measurements are performed with a receiver input power of -9 dBm. In Fig 3a, the only active scrambler is PS1 tuned on SR8 corresponding to 1.3°/ms average SOP-VS. Fig 3b is obtained by activating both PS1 (SR8) and PS2 (SR1000), leading to SOP-VS as fast as 110°/ms.

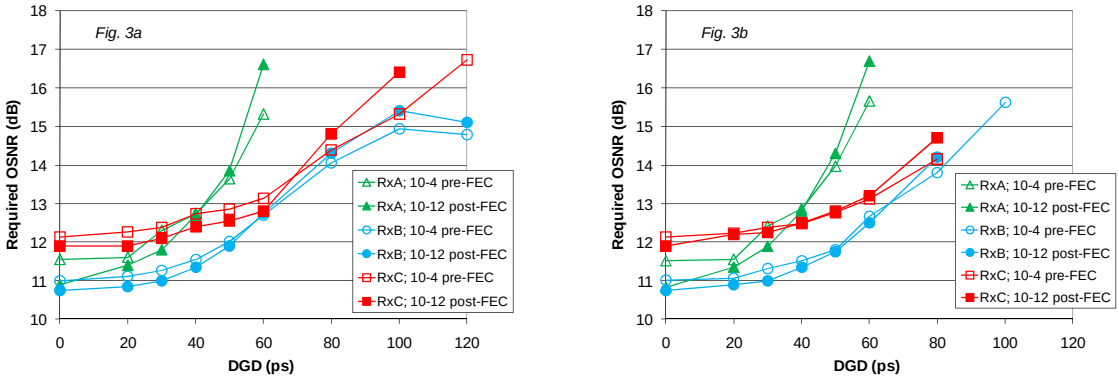

Fig. 3. Required OSNR versus DGD: a) 10^{-4} pre-FEC and 10^{-12} post-FEC with PS1 (SR8) and PS2 (0), b) 10^{-4} pre-FEC and 10^{-12} post-FEC with PS1 (SR8) and PS2 (SR1000). RxA: green triangles, RxB: blue dots, RxC: red squares. Empty symbols: pre-FEC, full symbols: post-FEC

In Fig. 3a, we observe that RxA is limited to a DGD tolerance of 60 ps, while RxB is robust to at least 120 ps. RxC cannot accept more than ~100 ps as synchro loss occurs for higher DGD levels. When considering 80 ps DGD, the required OSNR is quasi-similar for RxB and RxC even if it appears that penalty is a bit lower for RxC for the various DGD values. Finally, in Fig. 3a we observe that post-FEC penalties (at 10^{-12}) are lower than pre-FEC ones (at 10^{-4}) for low DGD values and becomes higher for high DGD. Fig. 3b compares the required OSNR at post-FEC 10^{-12} and pre-FEC 10^{-4} with 110°/ms maximum SOP-VS. Even if the performance of each receiver is identical up to a certain amount of DGD, we see that a rapid polarization scrambling results in synchro loss for high DGD values.

The evolution of pre and post-FEC BER as a function of the maximum value of SOP-VS (for different configurations of PS1 and PS2) has been plotted for RxB and RxC in Fig. 4a and Fig. 4b, respectively. Note that our equalizers are used in their standard configuration without any specific tuning. For each DGD value, OSNR is chosen in order to have a post-FEC BER close to 10^{-12} for the lowest scrambling speed.

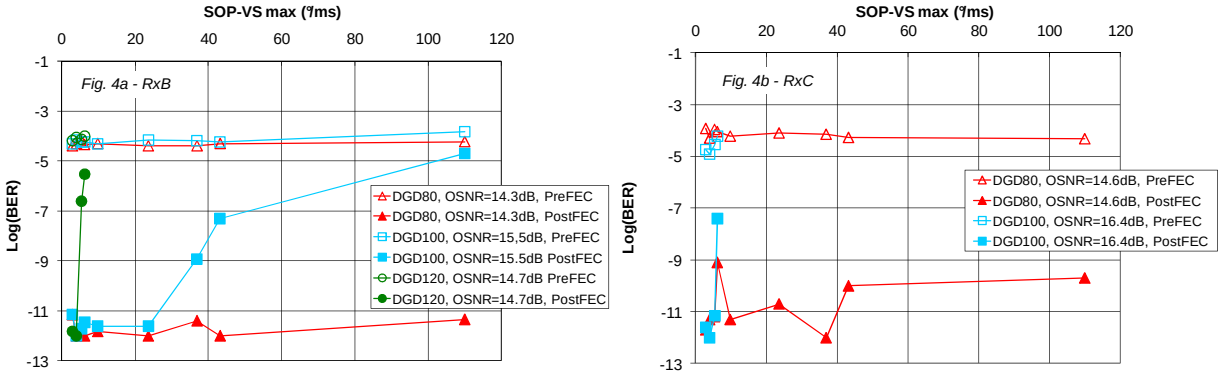

Fig. 4. Evolution of BER according to SOP-VS max. for a) RxB, b) RxC. Empty symbols: pre-FEC, full symbols: post-FEC

We observe on Fig. 4 that increasing the SOP-VS under a fixed DGD does not really impact the pre-FEC BER. It is not the case for post-FEC BER (ex: DGD=100 ps with RxB Fig. 4a): indeed, the FEC performance is affected by DGD and SOP-VS increase. Using Enhanced-FEC could improve the robustness against these effects but reference [4] in which E-FEC was used reports also this phenomenon. This is of particular importance when determining the engineering rules of transmission systems (as in [8]). Moreover, we see that the highest tested SOP-VS (compliant with values measured in the field [5]) lead to a reduction of about 20% of the amount of supported DGD for the two receivers under test. However we wonder if the reduction of the performances is not higher for RxB configuration as tolerance higher than 120 ps has already been reported for such kind of device. This should be further analyzed.

However with both solutions we obtain a significant improvement of the PMD that can be supported by the link (up to 25 ps PMD if we consider only first order (DGD) with unavailability of $1x10^{-5}$), which is significantly better than the gain brought by a traditional margin exchange [8]. These results should be further confirmed with higher order PMD tolerance tests but preliminary tests with 900 ps^2 SOPMD (DGD=80 ps) show negligible penalty.
As the OSNR obtained at the end of the link is around 18 dB, we have still ~ 3 dB OSNR margin under 25 ps PMD and 110°/ms SOP-VS after the 1000 km transmission line using MLSE-based equalizers and RS (255, 239) FEC.

5. Conclusion

We have presented some performance comparison results of two types of 10 Gbps MLSE-based receivers. It appears that the 16-state MLSE leads to the highest maximum DGD tolerance. The combination of a 16-tap FFE and 8-state MLSE is also a good alternative. In light of our results we can conclude that several 10 Gbps PMD compensation solutions able to cope with PMD as high as 25 ps and SOP variations as fast as 110°/ms are commercially available.

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