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Efficient Frequency Domain Chromatic Dispersion Compensation in a Coherent Polmux QPSK-Receiver

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Abstract: We investigate frequency domain chromatic dispersion equalization in an ASIC for digital coherent signal processing. Improved chromatic dispersion tolerance can be achieved by using modified coefficients, which utilize the equalizer more efficiently.

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1. Introduction

Upgrading of existing 10G systems with 40Gb/s and 100Gb/s coherent polarization multiplexed QPSK (CP-QPSK) systems is greatly simplified since linear impairments like chromatic dispersion (CD) and polarization mode dispersion (PMD) can be compensated within the digital signal processor (DSP). Classic CD-compensation with dispersion compensating fiber (DCF) may disappear in future links due to the enormous CD-tolerance of coherent receivers. But these capabilities come with the drawback of power consuming and complex DSPs. Thus efficient usage of the DSP-capabilities is necessary in order to keep power consumption and cost as low as possible.
Fig. 1a) shows a general architecture of a coherent receiver. A digital representation of the optical field is available after coherent detection and analog-to-digital conversion (ADC). Line synchronous sampling is achieved by using a digital clock recovery. In the following the linear fiber impairments are equalised. It is useful to do this separately for CD and for PMD, as CD is quasi constant with a large impulse response whereas PMD is a dynamic effect requiring a short impulse response for compensation [1,2].

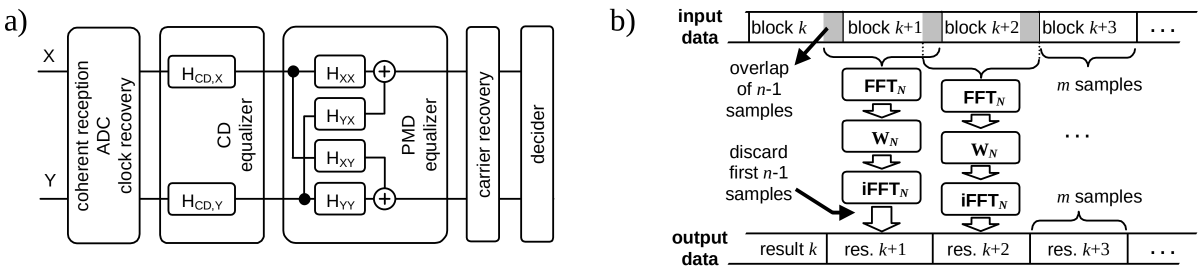

Fig. 1: a) Coherent CP-QPSK receiver architecture with separate CD and PMD equalizer filter. b) Schematic of overlap-save implementation of CD-equalizer with *n* taps and FFT-length *N*.

2. Frequency domain equalizer vs. time domain equalization

In general the CD equalizer consists of a finite impulse response filter (FIR) with *n* complex tap weights for each polarization. In a time-domain equalizer (TDE) the required number of taps *n* is defined by the maximum tolerable amount of CD. However for large numbers of *n* it is more efficient to use a frequency domain equalizer (FDE) that performs the filtering in the frequency domain e.g. by using the overlap save method as depicted in Fig. 1b). The incoming data is transformed with a fast Fourier transformation (FFT) of length N=n-1+m samples, where n-1 samples are part of the last data block and *m* samples are of the current block. Then the FFT result is multiplied with a frequency representation W_N of the filter impulse response and finally the data is transformed back to the time domain with an inverse FFT. The overlapping for n-1 samples is necessary to overcome the cyclic properties of the FFT. In a consequence the first n-1 results of the iFFT have to be discarded as well. The results of the FDE are mathematic identical to the ones of the TDE, but the complexity is much lower for larger numbers of *n* [3].

FFTs with lengths of powers of 2 can be implemented very efficiently using several methods like radix 2, radix 4, mixed radix or split radix. Radix 4 and mixed- split-radix are advantageous in an ASIC-implementation due to lower complexity and less latency. For simplicity, however, we concentrate only on radix 2 implementations. The number of required complex multiplications for a radix 2 FFT of length *N* is $(N/2)\log_2(N)$ [3]. If we implement a complex multiplication by using 4 real valued multiplications and 2 additions the required number of real multiplications is $2N\log_2(N)$. Note that inside the FFT all multiplications are performed with constants. On average about half of the bits which represent the twiddle-factors are zero, which results in a huge reduction of complexity after synthesis of an ASIC design. In a conclusion the number of real-valued multiplications for a single FFT can effectively be estimated to $N\log_2(N)$. Additionally to the forward and inverse FFT, N complex or $4N$ real-valued multiplications are necessary in the FDE. Synthesis does not reduce the gate-count here as the multipliers have to be designed for arbitrary filter settings. Therefore the complete FDE requires $2N\log_2(N)+4N$ real multiplications per polarization to calculate m output samples. Fig. 2a) shows the number of required real multiplications per output sample for n=65 and different FFT-lengths N. It reveals a minimum of ~25.2 real multiplications per output sample with an FFT-length of 2^9=512. The complexity increases moderately for higher numbers of N. For comparison: A TDE would require 4·65=260 real multiplications. Fig. 2b) compares the number of required multiplications of a TDE implementation with an FDE with optimized FFT-length N. Surprisingly the FDE is less complex already with 4 and more taps under the given assumptions.

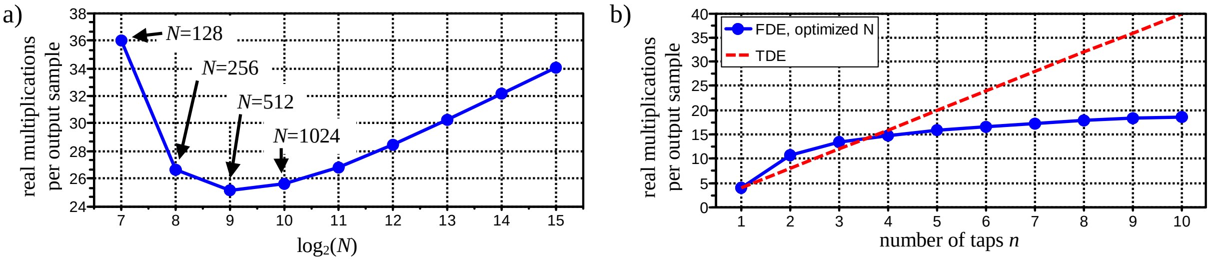

Fig. 2: a) Multiplicative complexity of 65-tap frequency domain equalizers with varying radix 2 FFT size. b) Comparison of frequency- and time-domain equalizer with respect to the number of required real multiplications per output sample

3. Chromatic dispersion compensation

The effect of pure chromatic dispersion can be described as an all-pass filter with a quadratic phase component. The corresponding tap-weights of the FIR-filter that compensates for the CD can be found by calculating the inverse Fourier transformation of the inverse CD transfer function in the required signal bandwidth (+/-10GHz for a 10Gbaud system). The length of the impulse response increases with increasing amount of CD. If the desired impulse response is longer than the number of taps that are implemented in the FIR filter, the impulse response has to be constrained to the filter length by truncation. The FDE performs a convolution which is effectively a correlation of the block data with shifted instances of the constrained, time-inversed impulse response. This is illustrated in Fig. 3a) for a CD-amount of 30,000ps/nm in a 43Gb/s CP-QPSK system and n=65 filter taps: The first sample in the output block of the FDE is the correlation of the block-data with the left-most shifted impulse response. The following output samples are generated by sequentially shifting the impulse response within the block until it finally reaches the right-most position. A significant improvement of the CD compensation performance can be achieved if we do not limit the impulse response to the 65 filter taps but use the whole length of the FFT (N samples), which we call the unconstrained filter impulse response. Fig. 3b) shows the resulting convolution process for this case. The output sample in the center of the block is now the result of the correlation of N data samples with the impulse response of length N and is therefore almost perfectly equalized. Towards the left and right ends of the block cyclic wrapping of the impulse response occurs. This leads to partly non-physical correlation with shifted data that leads to noise in the FDE result.

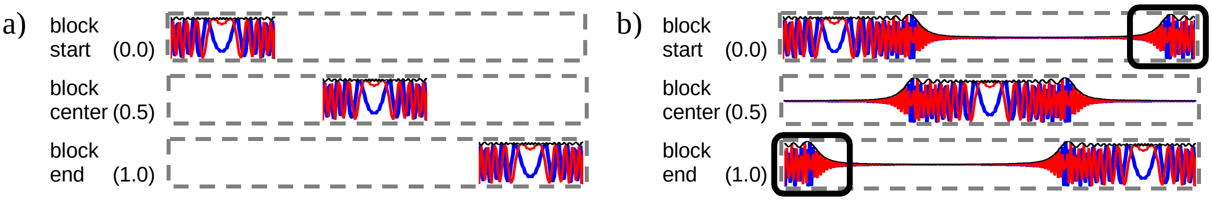

Fig. 3: a) Convolution using FFT and constrained impulse response. b) Convolution using FFT and unconstrained impulse response. Highlighted is the non-physical convolution of data with parts of the impulse response.

In order to visualize the reason for the improved performance of the unconstrained filter setting, we simulated data without applying optical noise. Fig. 4a) shows the averaged mean-squared-error (MSE) of the filter output calculated by comparing against the expected output sequence while compensating for 10,000ps/nm CD. All filter types show the same averaged MSE of ~-26dB in the whole processing block. Fig. 4b) shows the same signals for a CD of 20,000ps/nm. The MSE of the constrained/TDE filter setting increases to -18dB and is constant over the block-length. The unconstrained FFT-equalizers retain the good MSE value in the middle of the block. However, the

MSE increases at the block edges, where the cyclic property of the FFT generates excess noise from the non-physical convolution. At the start and end of the block the MSE has about the same value as with the constrained/TDE setting. The region with high MSE shrinks with increasing FFT-length. Fig. 4c) shows the results for 30,000ps/nm. Here the FFT128 equalizer is not able to achieve the back-to-back performance even in the center of the block but it has on average still a lower MSE compared to the TDE.

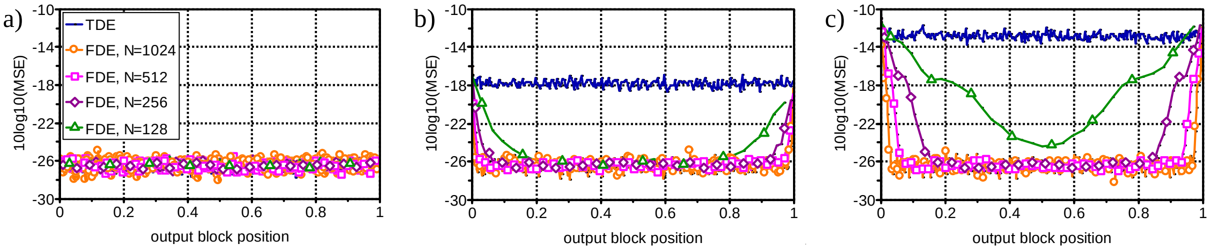

Fig. 4: Mean-squared-error (MSE) of equalizer output with noise-less input signal and chromatic dispersion of a) 10,000ps/nm, b) 20,000ps/nm and c) 30,000ps/nm. While the TDE output noise is constant over time, the FDE output noise shows variation over the block-period. Regions of worse performance shrink with increasing FFT-length.

4. Simulation results

We simulated 43Gb/s CP-QPSK data with varying amount of chromatic dispersion and processed the data using coherent receiver algorithms (Fig. 1a)). Fig. 5a) shows the resulting OSNR penalty over CD comparing the constrained and unconstrained CD-equalizer setting and using different FFT-lengths for a bit error ratio (BER) of 1e-3. The CD-tolerance at 0.5dB penalty of the constraint setting/TDE is ~20,000ps/nm. The tolerance extends by using an FDE with unconstrained filter setting. Moreover the CD-tolerance increases with the FFT-size while keeping the amount of overlap (*n*-1) constant. The 0.5dB penalty tolerance is 32,000ps/nm, 37,000ps/nm 43,000ps/nm and 47,000ps/nm for the FDE with *n*=65 and an FFT length of 128, 256, 512 and 1024 respectively. Fig. 5b) shows waterfall curves of the FFT512 equalizer with different amounts of CD. It reveals that with increasing chromatic dispersion the equalizer shows increasing penalties at lower BERs finally resulting in an error floor of ~2e-4 with 45,000ps/nm CD. Although simulations of 43Gb/s data has been presented, the results are in general valid for higher data rates, if filter size and FFT lengths are scaled quadratically with the bit rate.

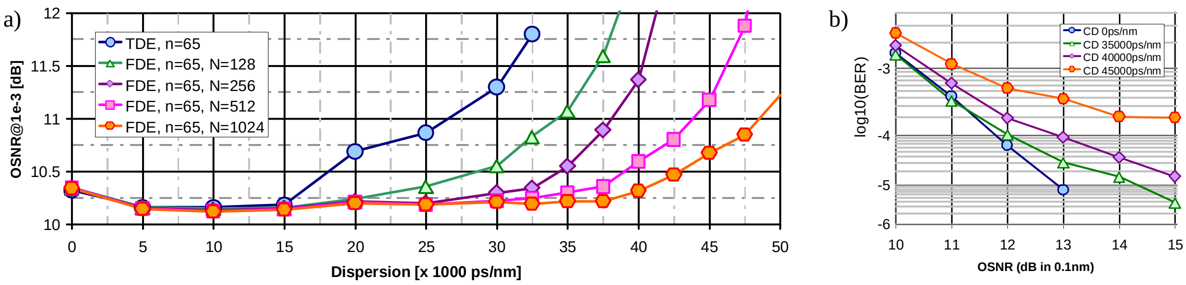

Fig. 5: a) Required OSNR for BER 1e-3 over chromatic dispersion of 65-tap FIR filter and 65-tap FFT filters with different sizes. b) Waterfall curves for 65-tap FFT512 equalizer with varying chromatic dispersion

6. Conclusion

We discussed the complexity of a frequency domain equalizer with a static filter with assumptions that are present in an ASIC design. FIR filters with a tap count of 4 and above could be more effectively implemented in the frequency domain and the FFT-length should be optimised to achieve the best efficiency. Furthermore we showed, that an unconstrained filter design has advantageous over the constrained method. An increase in CD-tolerance at BER1e-3 of >100% compared to the constrained method is possible when using longer FFT-sizes.

7. References

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