A 30 GHz Bandwidth, 80 GS/s Sample Rate Real-time Waveform Digitizing System

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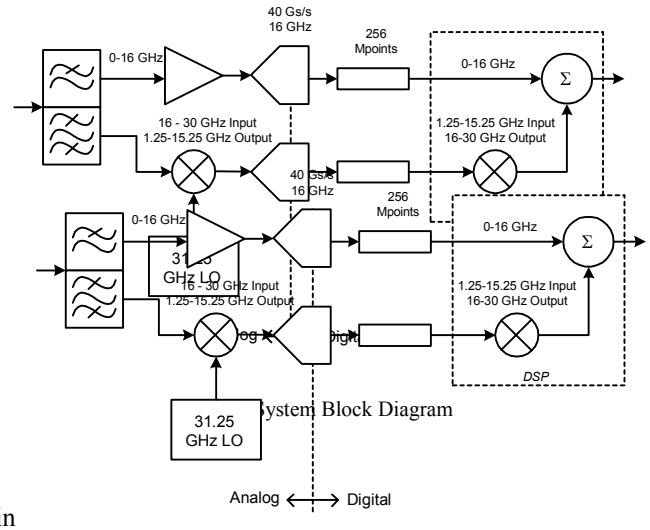
Abstract: A method employing a unique mixture of microwave and digital signal processing is described that provides for large bandwidth increases in waveform digitizers. Such digitizers are a critical component of 100+ Gb/s optical transmission systems.

1. Introduction

Optical communication systems operating at baud rates above 100 Gb/s employ complex modulation schemes such as DPM-QPSK and higher order modulation [5]. The receivers in such systems digitize the electrical signal at the output of an optical detector and process the waveform digitally to remove affects such as chromatic dispersion and PMD. Additional DSP is used to improve signal to noise and for equalization. Baud rates on a single polarization can exceed 28 Gb/s so the digitizer bandwidth requirements, assuming NRZ coding, extend to nearly 30 GHz.

This paper demonstrates a new method that has been utilized to create the fastest real-time waveform digitizer to date. The new method, called Digital Bandwidth Interleaving (DBI) utilizes microwave and digital signal processing (DSP) methods to double the bandwidth of existing architectures by employing a microwave front-end, and a DSP back-end [1]. The digitizer described here provides a bandwidth of 30 GHz with a sampling rate of 80 Gs/s.

This paper describes this new method and the details of how such a high-performance real-time waveform digitizing system was designed and built.



System Block Diagram

2. Basic Architecture

A DBI architecture is shown in Fig. 1. In this design, two 16 GHz, 40 GS/s digitizers are combined with a microwave front-end and a DSP back-end.

The microwave front-end consists of a diplexer that separates the incoming signal into two frequency bands feeding a down-converter to frequency translate the high band down to a frequency range suitable for acquisition by the ADC. Note that for the low frequency band, no down-converter is employed and for the high frequency band, a down-converter is employed but no front-end dc-amplifier is employed. For the high-frequency band, the down-converter module has digitally controllable gain adjust and the usable band does not extend to DC. Using only the ADC in the high frequency band reduces cost and lowers noise.

The down-converter consists of variable attenuation, a mixer, a local oscillator (LO), image reject filters and fixed gain amplifiers. The LO is derived from the A/D sample clock so that its phase is preserved in the sample timing.

The down-converter is driven by a LO that is set 1.25 GHz higher than the edge of the frequency band. In this way, the input to the down-converter is translated down and flipped over in frequency (i.e. high-side down-conversion is employed).

In this discussion, the following nomenclature is used to refer to the bands:

- LF - low frequency band - DC to 16 GHz
- HF - high frequency band - 16 to 30 GHz

On the DSP side, processing is performed to regenerate the input signal from the two 40 GS/s acquisitions. The recombination involves upsampling from 40 to 80 GS/s, digitally synthesizing a phase-locked rendition of the LO, up-converting the signal back to its original frequency band, rejecting unwanted images, and combining the results. The final result is a 30 GHz, 80 GS/s waveform acquisition.

3. Down-Converter

A detail of the downconverter is shown in **Fig. 2**. The first task of the downconverter is to provide variable attenuation such that the signal provided to the high linearity mixer is at a constant maximum level of -9 dBm, set 24 dB down from the LO for maximum mixer spur levels of -41 dBc.

There are additional filters placed before and after the mixer. The initial filter is designed so that no signal in the IF band of approx. 1.25-15.25 GHz is present at the RF port, otherwise the poor (approx. 15 dB) port-port isolation of the mixer causes spurs in the IF. The final filter is designed to reject mainly the LO that leaks to the IF port at about 0 dBm – this would saturate any downstream amplifier.

The fixed gain IF amplifier at the final stage sets the final output power to -4 dBm, which represents almost the full-scale range of the ADC (reserving 3 dB for digital compensation).

The LO is derived from the A/D sample clock which simplifies the generation of the LO in the DSP back-end processing. Temperature compensation is used to maintain the phase between the A/D and down converter LO.

The gain/attenuation of the downconverter is finely balanced such that the noise level never exceeds -49 dBc/GHz (giving a final SNR contribution of approximately 37 dB) and the spur levels never exceed -40 dBc, with the largest contributor being the IM32 of the final fixed gain amplifier. The final fixed-gain amp is a high power amplifier (OIP3 > 30 dBm, driven at 2 dBm max). The unit achieves typically in excess of 27 dB SINAD (4.5 ENOB).

4. Digital Signal Processing

Once the downconverted signal, along with the LF baseband signal are acquired by the two 40 GS/s digitizers and stored in high-speed memory, the waveforms are read out and processed through the DSP processing as shown in Fig. 3.

All signals undergo an interleave correction filter. Then, an adaptor, upsampler and fractional delay filter. The adaptor handles integer sample propagation time differences and the fractional delay handles the fractional sample time differences. The path propagation time differences are calibrated and stored in the instrument during factory calibration.

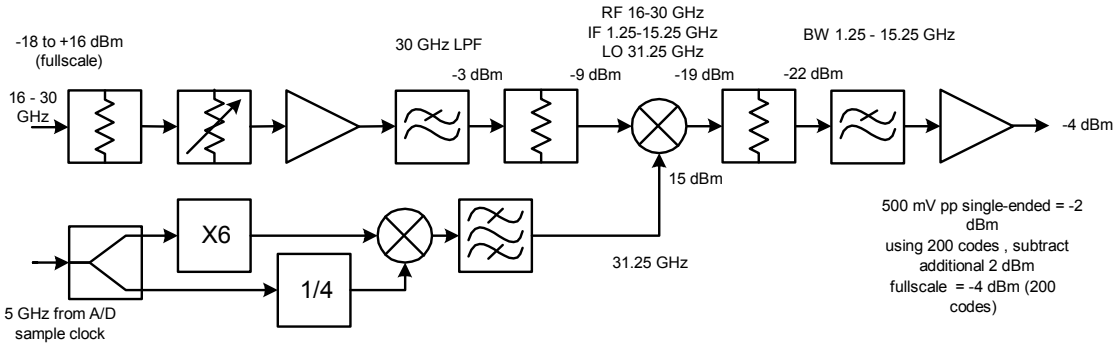


Fig. 2 - HF Band Down-Converter Block Diagram

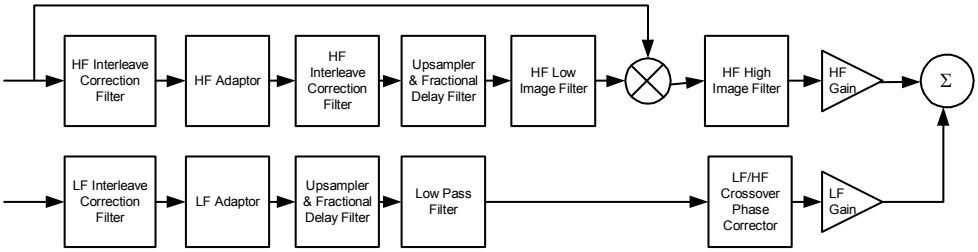


Fig. 3 DSP Processing Block Diagram

The upsampler is required because mixing of the signal will cause images that, if not upsampled, will alias into bands of interest. The mixing action is accomplished by generating a digital tone at the original LO frequency of 31.25 GHz. This digital LO is always in phase with the one used in the downconverter because the original LO was derived from the A/D sample clock. The LO is then mixed with the high band signal and the high image filters keep only the desired image.

Prior to summing the high band signal with the low band signal, it undergoes phase correction. This phase correction is a crude allpass filter applied to ensure that the signals at the band edges sum essentially constructively.

A gain adjustment is applied to rescale the signals to the same amplitude and the waveforms are summed.

The resultant signal is then compensated, first in magnitude, then in phase to produce a 30 GHz, 80 GS/s waveform acquisition.

The most important element in the DSP processing system is the magnitude and phase compensation system [2]. The raw and compensated magnitude response for a given gain setting is shown in **Error! Reference source not found.** where the typical maximum correction of -2 to +5 dB correction is shown. The magnitude correction is achieved using infinite impulse response (IIR) filters designed through pole/zero fitting with up to 100 poles and zeros.

The phase or group delay compensation is as important as the magnitude compensation. The phase compensation is achieved through filters designed using inverse Fourier transform (IFFT) techniques [3, 4].

5. Performance

The waveform digitizer described above has been used to demodulate optical signals at 56 Gbaud. The experiment described in [5] employed a set of four 30 GHz DBI digitizers in an optical receiver. The experiment demonstrated optical transmission over 2500 km with a BER of $< 2x10^{-3}$ at a rate of 224 Gb/s on a single optical wavelength.

6. Conclusion

The design of a 30 GHz, 80 GS/s digitizing system utilizing an RF downconverter at the front-end and DSP recombination at the back end has been shown. This design makes heavy use of DSP magnitude and phase compensation, without which, a high fidelity waveform acquisition would not be possible. The level of compensation required for use in an optical receiver could be considerably less since the goal is detection of a signal and not measurement of the signal characteristics. Reduced levels of compensation will also reduce the signal processing burden thus allowing for real-time implementations.

REFERENCES

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