Economics of 100Gb/s Transport

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Abstract: Deploying spectrally-efficient 100Gb/s coherent transponder technology in carrier networks can yield substantial CAPEX and OPEX savings. This paper discusses these economic gains and how a carrier can maximize their return on optical transport investment.

OCIS codes: (060.2330) Fiber optics communications; (060.4250) Networks

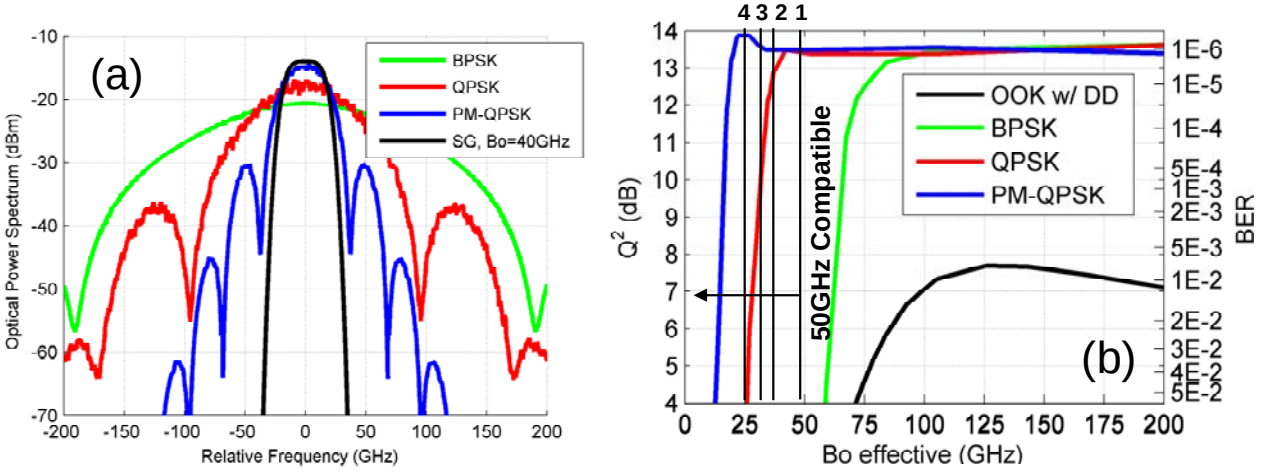
1. Introduction

The development of 100Gb/s transponder technology is rapidly progressing to meet the needs of carrier next-generation optical/IP networks. Video-driven IP traffic growth continues apace [1] with the need for ever higher speed ports on IP routers, Ethernet switches and OTN cross-connects driving the requirement for cost-effective client and line side 100Gb/s transponders. The key challenges clearly articulated by carriers across the globe is that 100Gb/s transponders must be deployable using 10Gb/s link engineering rules over existing fiber/DWDM infrastructure. The advent of coherent Dual Polarization Quadrature Phase Shift Keying (DP-QPSK), see Figure 1, with Electronic Dispersion Compensation EDC [2] clearly makes this possible, although the complexity of the electronics and photonics is substantial as compared to previous generation DWDM transponders. For mass adoption, the key challenge is how do we make this technology low cost? This invited paper will show how we can achieve aggressive cost points for 100Gb/s transponders and drive significant CAPEX and OPEX costs out of service provider networks.

2. Technology

Modulation and Coding

Increasing the data transmission rate from 10Gb/s to 100Gb/s whilst maintaining the same link engineering rules clearly necessitates some changes in modulation format and coding techniques. This requires a 10x improvement in OSNR sensitivity, PMD tolerance and spectral efficiency and a 100x improvement in CD tolerance. The use of coherent DP-QPSK is an elegant way of combating CD and PMD as the electromagnetic phase information is mapped from the optical to electrical domain using coherent detection, allowing electronic compensation of dispersive effects in DSP. By coding 4 bits per symbol, DP-QPSK also allows transmission through 50GHz optical filters. Indeed, the EDC also aids the spectral efficiency by combating narrowband filtering effects caused through multiple cascaded ROADMs by adjusting the equalizer tap weights to compensate the filtering effects. This allows 100Gb/s DP-QPSK to typically transit through as many as 10 cascaded ROADMs supporting 50GHz channel spacing. The spectral efficiency and optical filtering tolerance for DP-QPSK as compared to OOK, BPSK and QPSK is shown in Figure 2(a) and (b).



(a) Optical Spectrum (b) Optical Filtering Tolerance

Figure 2. Spectral Efficiency of 100Gb/s Modulation Schemes

It can be seen that 100Gb/s DP-QPSK offers a narrow spectral width that fits within a 40GHz width optical filter and that it offers tolerance to narrowband optical filtering (to < 25GHz FWHM). This enables transmission through multiple 50GHz ROADM filters, critical for real world network deployments.

As can also be seen from Fig.2(b), the Q is approximately 6dB higher for DP-QPSK vs OOK. This does not meet the necessary 10dB performance improvement needed to deploy using 10Gb/s OOK rules. The use of soft decision FEC [3] adds another 2-3dB improvement in Q, allowing 100Gb/s DP-QPSK with SD FEC to be deployed with design rules very close to 10Gb/s OOK. This minimizes the need for OEO regeneration in the network. Migrating to 100Gb/s brings significant economic gains related to: (i) 10x spectral efficiency gain vs 10Gb/s (or 2.5x gain vs 40Gb/s); (ii) OPEX gain due to reduced power consumption/bit and higher density/bit; (iii) IP efficiency due to fewer link aggregation (LAG) pipes [4].

3. Cost

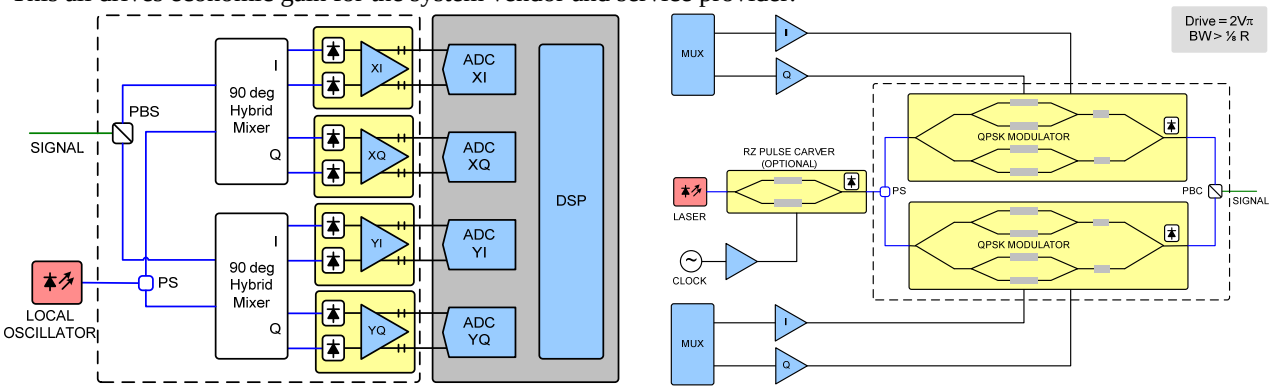
The performance advantages of coherent transmission and SD FEC facilitate straightforward deployment of 100Gb/s channels into existing carrier networks designed for 10Gb/s wavelengths. However, this modulation format and advanced coding technique adds considerably to the transponder design complexity. As complexity can often lead to added cost through higher number of components and manufacturing yield issues, an important design constraint is how to meet the market cost targets. To achieve the cost targets, the use of electronic integration and photonic integration can be implemented to reduce component count and improve manufacturability. The integration of OTU4 OH processing, SD FEC, DSP, firmware and control loops really creates a 100Gb/s line side "system in a module" concept, where other external components such as ASICs, optical compensators, optical amplifiers, etc. are not required on the transponder host board.

Electronic Integration

The monolithic integration of ADC, DSP and FEC in a single CMOS chip provides good cost reduction from high functionality concentrated into a single chip. It also removes the need for >Tb/s bus speed interconnect between ADC > DSP and/or DSP > FEC chips, which saves in space and power. By coding 4 bits/symbol this reduces the baud rate to a level that can be implemented in CMOS technology. This use of CMOS EDC rather than optical CD/PMD dispersion compensators saves considerable cost in reduced number of components and also in space and power. The use of SD FEC, approaching Shannon's Limit in terms of OSNR sensitivity, increases the optical reach which in turn reduces (or eliminates) the need for costly OEO regeneration and improves network economics.

Photonic Integration

The OIF is promoting standardization of the photonic integration for both the 100Gb/s transmit and receive optical sub-assemblies [5]. On the photonics transmit side, a single optical assembly contains the nested MZMs, PBS and splitters. On the photonics receive side, a single optical assembly houses the PBS, phase hybrids, balanced photodetectors and linear Trans-Impedance Amplifiers (TIAs). This OIF standardization has helped to create a supplier ecosystem around this technology, standardizing modulation format, module MSA footprint, electrical and control interfaces, Tx and Rx integrated photonics blocks. This concentrates R&D investment, brings a cost reduction through photonic integration and enables multi-sourcing at the integrated photonics and module level. This all drives economic gain for the system vendor and service provider.



(a) Transmit side Integration (b) Receive side Integration

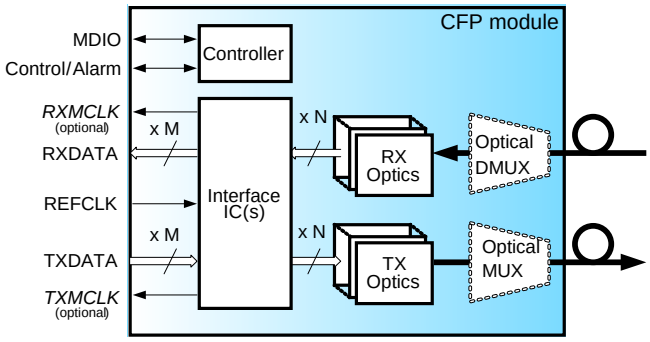
Figure 3. 100Gb/s Electronic/Photonic Integration.

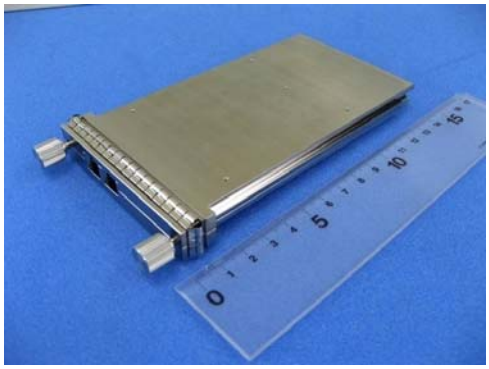
(The dashed enclosures in (a) and (b) indicate functionality defined in the OIF photonic integration projects)

4. 100G Client

The IEEE802.3ba working group has nearly completed their work on the standardization of 40Gigabit and 100Gigabit Ethernet. The proposed interfaces spanning copper media of 7m to single mode fiber media up to 40km all have adopted a parallelization of the bit stream. The single mode fiber applications specify four wavelengths each operating at either 10Gb/s for 40GBASE-R applications or at 25Gb/s for 100GBASE-R applications. For 100GBASE-R the wavelength spacing has been termed LAN-WDM or Local Area Network Wavelength Division Multiplexing.

The industry has been developing a number of module form factors to support the IEEE802.3ba draft interfaces. Module form factors such as the CFP MSA allow systems designers to speed up their design cycle, saving time and resources versus implementing a design with discrete components. Additionally, the definition of the CFP MSA slot creates a single system configuration which can be easily adapted to accommodate different reach and optical interface types. The CFP MSA has defined a module form factor which emphasizes flexibility with multiple pin-map configurations ranging from 3x XLAUI to OTL4.10. The pin-map flexibility leverages the current industry common denominator lane rate of 10Gb/s. This common lane rate simplifies the design of network system ASICs to interface to CFP and other modules for 40GbE and 100GbE applications.





(a) Functional Block Diagram (b) Mechanical Design

Figure 4. 100Gb/s CFP Client Module

5. Summary

The economics of 100Gb/s transport is being driven by ITU and IEEE standardization activities on both the client and the line side and Implementation Agreements defined by the OIF. This helps to focus R&D capital and creates an ecosystem supporting multiple suppliers, with a robust supply chain for 100Gb/s technology. Component integration in electronics (monolithic CMOS chips integrating ADC, DSP and FEC functionality) and photonics (OIF Tx and Rx optical assemblies) is driving very low cost points. Additional gains from 100Gb/s are realized by improved spectral efficiency and IP link aggregation. It is predicted that 100Gb/s technology will provide compelling economics for next-generation optical transport network deployments.

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