High Bit-Error Tolerant Frame/Lane Alignment for 100 Gb/s Multi-Lane Transmission

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Abstract:
We study high bit-error tolerant frame/lane alignment for 100 Gb/s multi-lane transmission with advanced modulation formats. Bit-error allowance/correction for frame/lane alignment improves the bit-error tolerance and achieves stable operation even at the uncorrected BER of 10^{-2}.

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1. Introduction

100 Gb/s transmission technologies are being studied extensively in step with the standardization of 100 Gb/s Ethernet in IEEE 802.3ba and the evolution of Optical Transport Network (OTN) in ITU-T. Various technologies are needed to realize high speed transmission: advanced modulation formats such as dual-polarization quadrature phase-shift-keying (DP-QPSK), digital coherent receivers, and high performance forward error correction (FEC). Advanced modulation formats include polarization multiplexing and multi-level modulation in order to relax the required bandwidth for various devices and to mitigate transmission impairment. These advanced modulation formats lead to multi-lane transmission. In the case of DP-QPSK, each wavelength has 4 lanes: X-pol I-ch, X-pol Q-ch, Y-pol I-ch, and Y-pol Q-ch (pol: polarization, ch: channel, I: In-phase, Q: Quadrature-phase). Digital coherent technology realizes, for example, polarization de-multiplexing, and the compensation of chromatic dispersion by using digital signal processing (DSP). Furthermore FEC with soft decision and increased redundancy, near 20%, is being studied actively and the Shannon limit is being approached. Such an FEC code can improve the BER, for example, from 10^{-2} to 10^{-12}. These technologies are key enablers of 100 Gb/s transmission.

Figure 1 shows the configuration of a 100 Gb/s transmission system with the above mentioned technologies. The transmitter side uses a “lane distribution” block to distribute the single OTU frame among the multiple lanes. The receiver side has a “lane aggregation” block to aggregate the multiple data into the original OTU frame. As shown in the insets of Figure 1, a frame/lane alignment functionality must be set between the “lane distribution” block and “lane aggregation” block in order to distinguish each lane from the others, to detect skew between lanes, and finally to reconstruct the original OTU frames. This transmission system places the “FEC decoder” block after the “lane aggregation” block, so the “lane aggregation” block must work well at the BER before error correction. The higher performance FEC has, the worse the BER at the “lane aggregation” block is. Given the above consideration, frame/lane alignment in multi-lane transmission must operate, for example, at the BER of 10^{-2}.

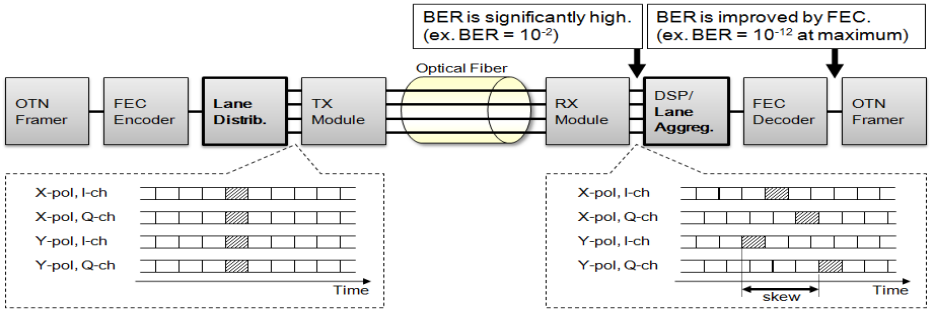

Fig. 1. Configuration of 100 Gb/s transmission systems with, for example, DP-QPSK modulation format. (Distrib.: distribution, Aggreg.: aggregation, DSP: digital signal processing, pol: polarization, ch: channel)

In this paper, we study high bit-error tolerant frame/lane alignment for 100 Gb/s multi-lane transmission. For multi-lane transmission, we adopt the OTUk multi-lane transport specified in ITU-T G.709 Annex C [1], which specifies OTUk transport via the 40GbE/100GbE optical module. We evaluated the frame/lane alignment performance by utilizing the method described in the literature [2]. Our evaluation shows improvement of the frame/lane alignment performance by using bit-error allowance and/or bit-error correction for frame/lane alignment related overhead. We investigate the parameters of bit error allowance and bit error correction in order to achieve operation at the BER of 10^{-2}.

2. Application of "OTUk multi-lane transport (G.709 Annex C)" to 100 Gb/s transmission

Key mechanisms of the OTUk multi-lane transport specified in G.709 Annex C are 16-byte data distribution and lane rotation. To support these mechanisms, each lane uses a frame alignment signal (FAS) and multi-frame alignment signal (MFAS). FAS bytes have the fixed bit pattern of "F6 28"; MFAS takes values from 0 to 255 and is incremented frame by frame. The 40GbE/100GbE optical module has 4 logical-lanes/20 logical-lanes, respectively. If the number of logical-lanes differs from that of physical-lanes, logical-lanes are bit multiplexed (demultiplexed) at the transmitter side (receiver side). At the receiver side, each lane is frame aligned by using FAS bytes and then lane aligned by using MFAS and/or 6th FAS byte as a lane marker. The lane marker is also used for the detection of skew between lanes. This specification is based on the BER of 10^{-4}, because it assumes the use of the standardized FEC, RS(255, 239).

We apply this mechanism to 100 Gb/s transmission with advanced modulation formats. As mentioned above, DP-QPSK has 4 lanes, so the use of 4 logical-lanes is adopted in our study. Data is distributed among 4 logical-lanes and then each logical-lane is transported using a different DP-QPSK lane. In the following section, we evaluate the frame/lane alignment performance and propose some techniques for improving the bit-error tolerance. Several parameters affect the performance of frame/lane alignment (Table 1). We assumes OTU4[V] frame with frame period of 1.168 μs. So each lane receives FAS/MFAS bytes every 1.168 x 4 = 4.672 μs.

Table 1. Parameters impacting frame/lane alignment.

Parameter	Description
p (bit)	Pattern length for alignment
c	Number of consecutive checks
e (bit)	Bit error allowance
ec (bit)	Bit error correction

Table 2. Average time to false frame alignment. (e0 means *e* = 0, etc. Unit: frames)

	e0	e1	e2
c2	1 x 10^{14}	1 x 10^{11}	5 x 10^{8}
c3	6 x 10^{23}	2 x 10^{19}	4 x 10^{15}
c4	3 x 10^{33}	2 x 10^{27}	3 x 10^{22}
c5	1 x 10^{43}	3 x 10^{35}	3 x 10^{29}

Table 3. Average time to false lane alignment. (ec0 means *ec* = 0, etc.)

	ec0	ec1
c1	8 x 10^{3}	4 x 10^{8}
c2	4 x 10^{13}	9 x 10^{22}
c3	2 x 10^{23}	2 x 10^{37}
c4	7 x 10^{32}	5 x 10^{51}

3. Frame alignment performance

Frame alignment has two states: in-frame (IF) and out-of-frame (OOF). ITU-T Recommendation specifies that IF is entered when valid 4-byte FAS (*p* = 32) is received twice in succession (*c* = 2) in the OOF state; OOF is entered when invalid 3-byte FAS (*p* = 24) is received five times in succession (*c* = 5) in the IF state.

Figure 2 shows the frame alignment performance considering the bit error allowance. At the BER of 10^{-2}, frame alignment is established in 2.3 frames on average with no bit error allowance (*e* = 0) and (*c* = 2). At the BER of 5 x 10^{-2}, 30 frames (*c* = 2) or over 100 frames (*c* = 3) are required to establish frame alignment. 1-bit or 2-bit error allowance improves the frame alignment performance. One more thing that we have to consider is false in-frame. Bit-error allowance improves the performance, however, the probability that the expected pattern will be simulated by a random bit stream is increased. Table 2 shows the time to false in-frame in the unit of frames. (*e* = 1, *c* = 2) and (*e* = 2, *c* = 2) is fairly short. Increasing parameter *c* improves the false in-frame performance.

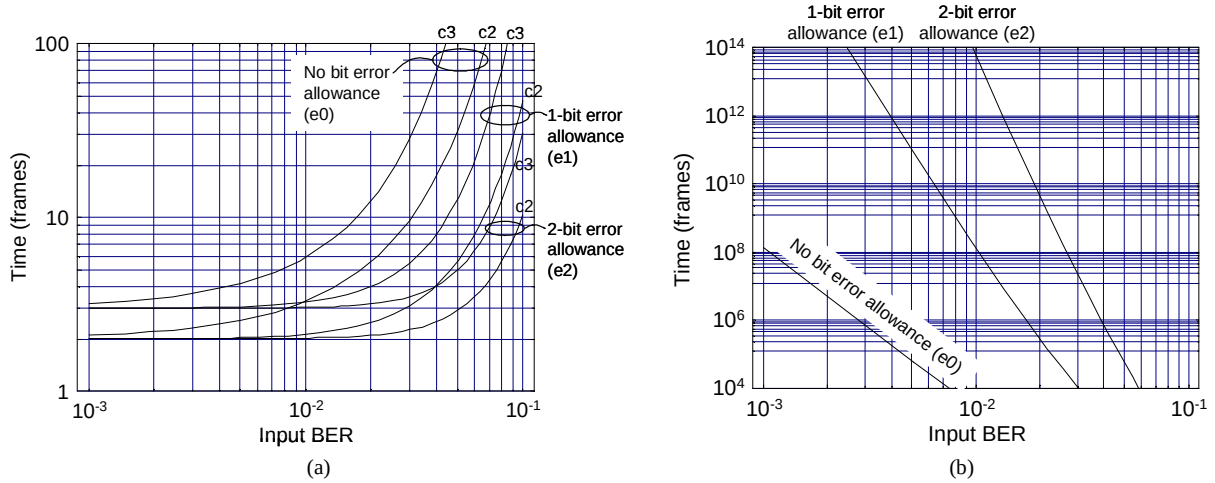

Fig. 2. Frame alignment performance with consideration of bit error allowance. (a) Average time to frame alignment establish and (b) Average time to out-of-frame alignment. (c2 means *c* = 2, etc. See Table 1).

Figure 2 (b) shows the average time to OOF. The parameter *c* is fixed to *c* = 5, which is the standard value. In the case of no bit error allowance, the time to the OOF at the BER = 10^{-2} is less than 10^{4} frames, which corresponds to

47 milliseconds. When 1-bit error is allowed, the time increases to about 10^8 (8 minutes), however this is not enough. 2-bit error allowance improves the time to about 10^{14} (15 years).

These evaluations indicate the following parameters for frame alignment is (e = 0, c = 2) or (e = 1, c = 3) for OOF to IF transition, and (e = 2, c = 5) for IF to OOF transition. These parameters can achieve robust frame alignment performance even at the fairly high BER of 10^{-2}.

4. Lane alignment performance

Lane alignment has two states similar to frame alignment: in-lane-alignment (ILA) and out-of-lane-alignment (OLA). ITU-T is now standardizing the lane alignment procedure. We assume ILA will be entered when a consistent set of MFAS is received in the OLA state; OLA will be entered when an inconsistent set of MFAS is received in the ILA state.

Figure 3 (a) shows the average time to the ILA state with consideration of bit error correction. Bit error correction of lane alignment related bytes can be realized by using, for example, Reservation byte(s) in the OTUk overhead area (Row 1, Column 13-14). At the BER of 10^{-2}, each set of parameters in the figure yields sufficient performance, though 1-bit error correction offers slightly better performance. The other thing we have to consider is false lane alignment similar to false frame alignment in the previous section. Table 3 shows that (ec = 0, c = 1) and (ec = 1, c = 1) have fairly short times to false lane alignment. If the time to false lane alignment should be more than 1 year, (ec = 0, c = 2) or (ec = 1, c = 2) are suitable. Figure 3 (b) shows the average time to OLA. At the BER = 10^{-2}, state transition from ILA to OLA will occur instantaneously when no bit error correction (ec = 0) is adopted. 1-bit error correction (ec = 1) with 5 consecutive checks (c = 5) improve the performance. 1-bit error correction (ec = 1) with 10 consecutive checks (c = 10) increase the time to around 10^{14}, which corresponds to 15 year.

As a result, parameters for robust lane alignment are (ec = 1, c = 2) for OLA to ILA transition, (ec = 1, c = 10) for ILA to OLA transition. The performance is decided by the combination of the parameters, so other parameters sets are also possible.

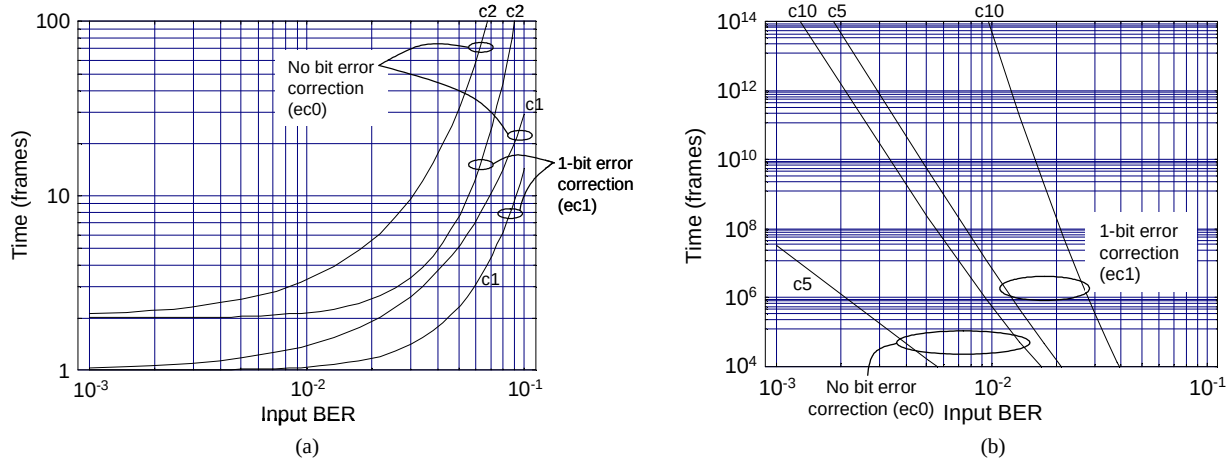

Fig. 3. Lane alignment performance with consideration of bit error correction. (a) Average time to in-lane-alignment and (b) average time to out-of-lane-alignment. (c1 means c = 1, etc. See Table 1)

5. Summary

We have studied high bit error tolerant frame/lane alignment for 100 Gb/s multi-lane transmission with advanced modulation formats. Bit error allowance and/or bit error correction for frame/lane alignment related overhead significantly improve the bit-error tolerance and enable operation even at the high BER of 10^{-2}. We conclude that our frame/lane alignment approach will achieve reliable 100 Gb/s system operation.

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References

[1] ITU-T Recommendation G.709 Amendment 3, Annex C, “Adaptation of OTU3 and OTU4 over multichannel parallel interfaces”.
[2] D. W. Choi, “Frame alignment in a digital carrier system – A Tutorial,” IEEE Communication Magazine, pp. 47-54, Feb. 1990.