Soft Decision FEC for 100G Transport Systems

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Abstract: A practical implementation of soft decision based FEC for 100G transport systems is discussed. The keys are a stronger coding gain using triple-concatenated FEC and a multi-lane distribution architecture to improve the error correction capability.

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1. Introduction

There has been a recent reawakening of interest in coherent optical receivers because a carrier-phase estimation method using digital signal processing for demodulation of multi-level coded signals is becoming promising for 100 Gb/s optical transport systems. Compared with 10 Gb/s optical transmission, we require 10 dB higher optical signal-to-noise ratio (OSNR) for 100 Gb/s transmission. No matter how excellent the performance of the digital coherent technology, the required OSNR for dual-polarization quadrature-phase-shift keying (DP-QPSK) is at best only 6 dB lower than that for on-off keying (OOK). Therefore, at least 4 dB coding gain enhancement over that for 10 Gb/s OOK is essential for realization of 100 Gb/s DP-QPSK transport systems. In order to address this issue, there is an increasing demand for powerful forward error correction (FEC) to improve the OSNR capability.

Fig. 1 plots the progress in FECs for optical communication systems over the past 20 years. The vertical axis shows the product of (linear) net coding gain (NCG) defined in terms of a post-FEC bit error ratio (BER) of 10^{-15} and bit rate in Gb/s. The three sets of data points represent the different FEC schemes: 1st generation FEC using linear block codes represented by RS(255,239); 2nd gen. concatenated codes; and 3rd gen. FEC based on soft decision and iterative decoding. A clear trend can be seen in that an improvement of 1.4 times has been achieved every year. This improvement has been achieved not by FEC algorithm improvements, but by large scale integration (LSI) technology evolution.

Several approaches for powerful FEC for use at 10 to 40 Gb/s have seen intensive development. For example, a Block Turbo code (BTC) LSI was reported with a Q-limit of 6.3 dB at 10 Gb/s [1], Optical transport network (OTN) compatible enhanced FEC (EFEC) LSI has been developed with a Q-limit of 9.1 dB at 43 Gb/s, which yields a BER below 10^{-12} [2], and two orthogonally concatenated Bose–Chaudhuri–Hocquenghem (BCH) codes, whose NCG is 10.1 dB with 25% redundancy is proposed [3]. However, no practical FEC LSI applied to the 100 Gb/s region and showing comparable performance has been seen yet. One of the reasons is that it is difficult to implement the algorithms in LSI in a fully parallel way with a practical circuit size. For example, while an infinite number of soft decision bits would yield ideal correction capability, circuit implementation would be impossible. A near-infinite number of iterations would yield superior error correction performance, but unacceptable latency would result. For 100 Gb/s optical transmission systems, the implementation of next generation FECs has been vigorously studied, *e.g.* low-density parity-check (LDPC) code with an optical channel transport unit-4V (OTU4V) frame structure [4], field programmable gate array (FPGA) implementation of G.975.1 FEC [5], and a variety of advanced FEC systems with iterative decoding, including a novel class of non-binary LDPC codes particularly suited for FPGA decoder implementation [6].

As another issue, we have to pay attention to signal degradations such as burst errors and phase slip caused by incomplete phase recovery algorithms for correcting phase noise accumulation in digital coherent systems. As a consequence, the FEC performance is affected, and it becomes a key issue to research robust FEC codes against the signal degradations of the specified PSK format. In order to improve the

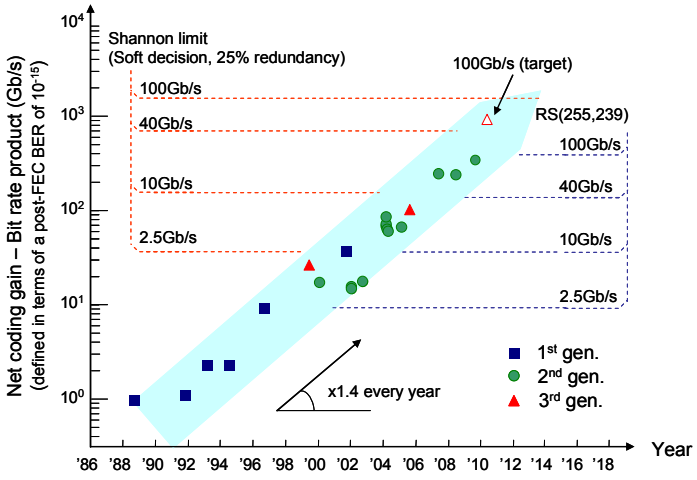

Fig. 1. Progress in FECs for optical communications.

error-correction performance, tracking the decision threshold is also essential. Automatic decision threshold tracking for 3-bit soft decision decoding has been demonstrated [7].

In this paper, we discuss the practical implementation of a soft decision based FEC for 100G transport systems. We developed FPGA boards for emulating soft decision FEC, and demonstrated the concatenation of a Reed-Solomon (RS) code and an LDPC code yielding a Q-limit of 7.1 dB [8]. As a more powerful FEC, we propose a triple-concatenated FEC. The concepts involved are: the concatenation of a pair of concatenated hard decision based block codes with soft decision based LDPC codes; approximately 20% redundancy ratio compliant with optical internetworking forum (OIF) standards, which results in a transmission rate of 120~130 Gb/s; and an OTU4V frame format compliant with ITU-T G.709.

2. FPGA Prototyping for Soft Decision FEC

To evaluate the FEC codes in hardware, we developed high-speed FPGA emulator boards. The board for the LDPC decoder is shown in Fig. 2. Two FPGAs fabricated in 90 nm were used for the FEC encoders (RS ENC and LDPC ENC); eight plus one were used for the FEC decoders (LDPC DEC and RS DEC). Since it was difficult to handle the whole 100 Gb/s Ethernet (100 GbE) signal with 20.5% redundancy in the FPGAs due to circuit size constraints, we used 31.3 Gb/s for the test, being a quarter of the full DP-QPSK signal.

Fig. 3 shows the experimental setup to measure the error-correction capability. A 2^{31}-1 pseudorandom binary sequence (PRBS) test signal at 10.3125 Gb/s from a 10GbE tester is input to the FPGA board. A gear box, which is a data rate changer using idle bits and high-speed memories, generates a container for the OTU4V frame at a rate of 12.5 Gb/s, and is followed by the outer RS ENC. We use three-stage interleaving (IL). After second-stage IL, the LDPC ENC calculates the redundant parity and the concatenated FEC-framed signal is generated.

The FEC-framed signal is interleaved at the third stage. The dummy PRBS bits are inserted in the OTU4V frame at a rate of one in four, such that the line rate becomes 15.6 Gb/s (12.5 x 5/4). This 15.6-Gb/s signal is duplicated and the signals are bit-multiplexed together. The resulting 256 parallelized quasi-FEC-framed signal at 31.3 Gb/s is time aligned by the preskew circuit based on a deskew alert from the receiving side. Then, it is multiplexed and converted to optical OOK by the $LiNbO_3$ Mach–Zehnder modulator (LN Mod). The OSNR is intentionally degraded by adding amplified spontaneous emission (ASE) as additive white Gaussian noise. The input Optical Channel (OCh) is regenerated and the 2-bit soft decision variables are input to the frame alignment circuit. After de-interleaving, iterative decoding of the LDPC code and RS decoding are achieved.

Fig. 2. FPGA board for emulating LDPC DEC.

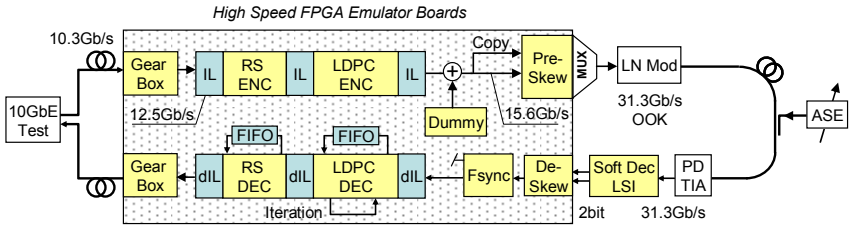

Fig. 3. Experimental setup for FEC performance evaluation.

3. Triple-concatenated Soft Decision FEC Scheme for 100 Gb/s Transport Systems

Fig. 4 shows the concept of our proposed triple-concatenated soft decision FEC for 100 Gb/s systems. To achieve an NCG of nearly 11 dB, we must optimize the combination of concatenating codes in terms of the higher BER region. In the conventional combination the residual error after decoding at an inner code is normally less than 10^{-4} to correct properly at an outer code including RS(255, 239) FEC compliant with G.975 (Fig. 4(a), (b)). Our approach is the application of LDPC as an inner code for the higher BER region (BER > 10^{-3}) and a powerful concatenated code as an outer code for the lower BER region (BER < 10^{-3}) as shown in Fig. 4(c), (d). LDPC shows good error correction performance for high BERs from 10^{-2} to 10^{-3}. If LDPC concentrates the error correction performance on this higher

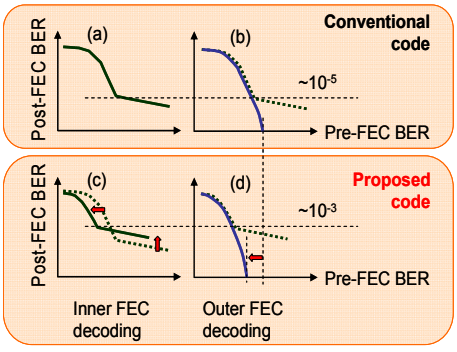

Fig. 4. Concept of proposed triple-concatenated soft decision FEC.

BER region, an increase in the residual BER floor is inevitable (Fig. 4(c)). In order to maintain the system performance, we combine powerful concatenated outer codes with the LDPC (Fig. 4(d)). The application of this triple-concatenated soft decision FEC has the following features: (1) the concatenation of a pair of concatenated hard decision based block codes having 7% redundancy with soft decision based LDPC codes; (2) approximately 20% redundancy ratio compliant with OIF standards, which results in a transmission rate of 120~130 Gb/s; (3) an OTU4V frame format compliant with ITU-T G.709; (4) straightforward circuit implementation via a well designed parallelized pipe-line architecture. We expect that the proposed concatenated codes can achieve an NCG of nearly 11 dB at a post-FEC BER of 10^{-15}, which is at least 2 dB better than that of a hard decision EFEC [2].

4. Circuit Implementation

Fig. 5 shows an example of a block diagram of an optical transceiver with digital coherent technology and triple-concatenated soft decision FEC. The optical transceiver consists of an OTU4 framer with a hard decision EFEC encoder/decoder as the outer codes and digital signal processor (DSP) with a soft decision LDPC encoder/decoder as the inner code. To reduce the circuit board complexity, we propose that the function of the soft decision LDPC be implemented in the DSP block. We have to note that inter-lane skew at the receiver side, which is caused by polarization mode dispersion (PMD), chromatic dispersion (CD) in transmission and nonlinear phase noise along an optical fiber, affects LDPC decoding performance. In order to address this issue, the multi-lane distribution (MLD) is also implemented in the DSP to compensate the skews and the lane switching. The number of lanes is four. This is because the DP-QPSK signal format has four channels that are dual polarized, in-phase and quadrature-phase. The FEC frame is constructed for each lane individually. The skews and the order of each lane do not affect the LDPC performance by separating the FEC frame. This shows that the FEC frame separation scheme along with the transmission lanes can overcome the undesirable impairment caused by incomplete data recovery in the DSP.

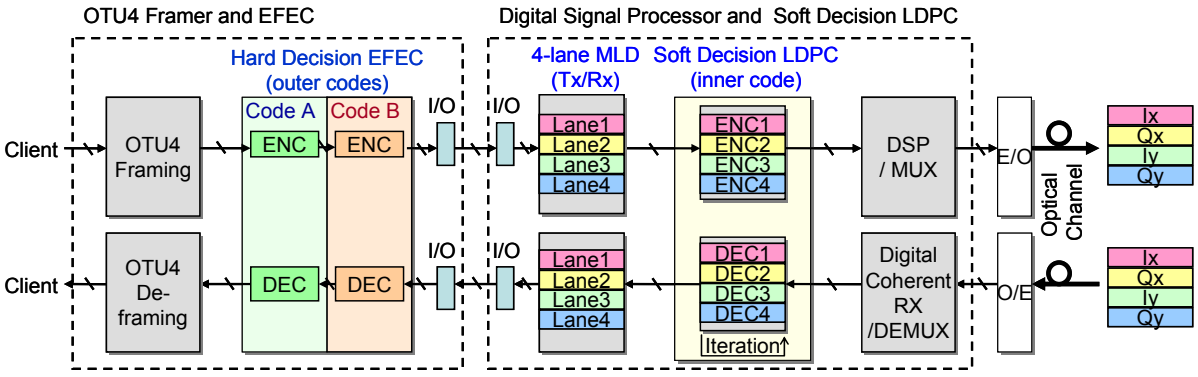

Fig. 5. Block diagram of optical transceiver for 100G transport systems.

5. Conclusions

We have discussed the practical implementation of a soft decision based FEC for 100G transport systems. We have developed FPGA boards for emulating soft decision FEC, and demonstrate the concatenation of an RS code and LDPC code. As a more powerful FEC, we have proposed a triple-concatenated FEC to reach an NCG of nearly 11 dB. We believe that the proposed concept of soft decision based triple-concatenated FEC and this implementation scheme will have a large positive impact on next generation 100G optical transmission systems.

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