Single-Chip All-Optical Packet Processor Based on All-Optical Flip-Flop Monolithically Integrated with MZI-SOA Switch

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Abstract: We fabricate and demonstrate all-optical packet switching using a single photonic integrated circuit (PIC), which is constructed from monolithically integrated all-optical flip-flop and switch. Both 10 and 40-Gb/s signal can be transmitted through the PIC.

OCIS codes: (130.3120) Integrated optics devices; (130.4815) Optical switching devices;

1. Introduction

All-optical flip-flop (AOFF) has been recognized as a promising device to enable intelligent all-optical signal processing, since it acts as an all-optical memory element in photonic integrated circuits (PICs) [1,2]. Various types of AOFF have been demonstrated with an ability of photonic integration with waveguide structure [3,4], however, none of them was monolithically integrated with other optical devices to our knowledge. Photonic integration is an attractive technique because it can reduce number of fiber-to-waveguide coupling, which is a major factor to determine optical loss. In addition, photonic integration reduces number of components and temperature controllers, which also results in reduction of power consumption [5].

We have proposed and developed an AOFF based on Multimode Interference (MMI) bistable laser diode (BLD) [6]. By using distributed Bragg reflectors (DBRs), the AOFF can be monolithically integrated since no cleaved facet is required for the operation. In this paper, we report, for the first time, a PIC with monolithically integrated AOFF and Mach-Zehnder interferometer (MZI) semiconductor optical amplifier (SOA) switch to perform single-chip all-optical packet switching. The AOFF acts as label memory in PIC to drive the switch. Since the switch is transparent to the data rate of payload, both 10-Gb/s and 40-Gb/s optical signals are switched successfully.

2. Concept and Device Design

Concept and timing chart of the all-optical packet switching is shown in Fig. 1(a) and (b), respectively. The PIC has five I/O ports. When set labels are injected to the PIC, payload signal are switched to an output port 2. The set label is latched in the AOFF to control the MZI-SOA, so that the switching state is maintained until release label injections. Since we can add set and release labels as headers and footers of the payload, variable length packets are available in this scheme. However, we divided the header set label and used it also as the release label with a delay line in this experiment. Since we use the MZI-SOA as a switch and original signal is transmitted through the output port, this scheme is transparent to the payload format.

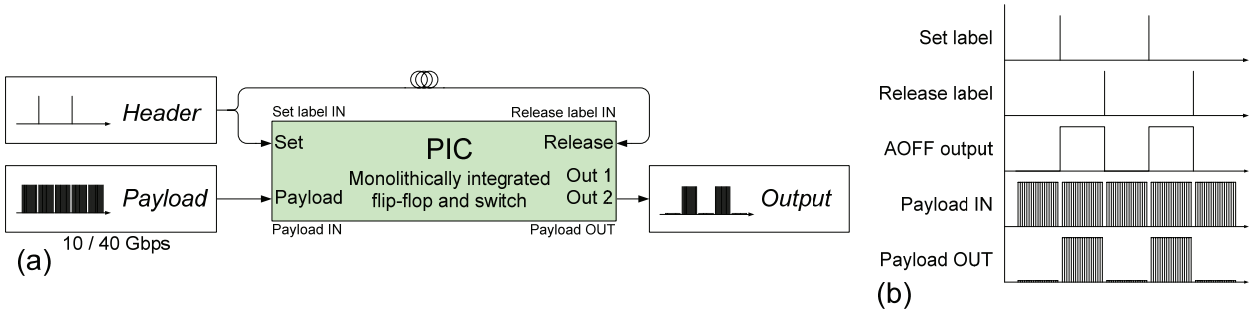

Fig. 1: (a) Concept of single-chip all-optical packet switching. Payload signal is switched to output port 2 from set label until release label injection. In order to use simple setup, we divide header signal and use it as both set and release label after a delay line. (b) Timing chart of the single-chip all-optical packet switching. Set labels are latched in the AOFF to drive the switch.

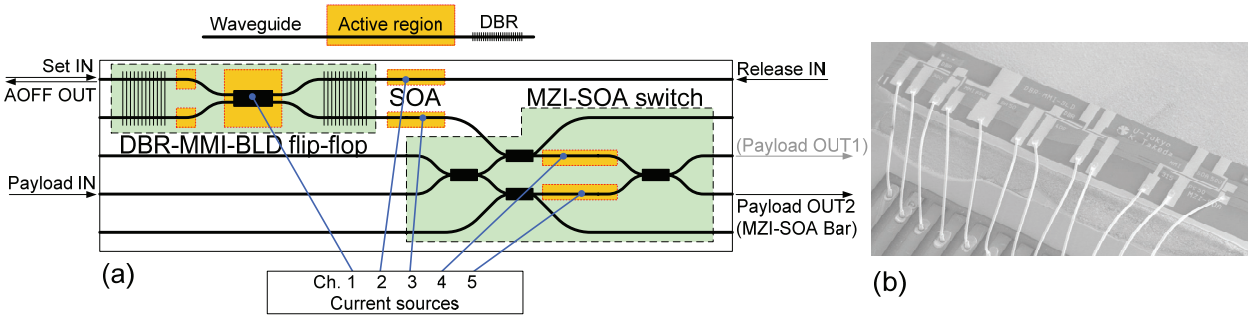

Fig. 2: (a) Schematic of the PIC. Black solid lines and orange region correspond to waveguides and active region, respectively. Connections of current sources are shown in blue line. (b) SEM image of the fabricated device.

A chip layout is schematically shown in Fig. 2(a). We used a DBR-MMI-BLD as the AOFF. Design of AOFF was same as described in [7]. The operation principle of the flip-flop is based on two-mode bistability in the 2×2 active MMI cross coupler with cross gain saturation and saturable absorption, as described in [8]. We used an MZI-SOA as the all-optical switch, which was constructed from two 2×2 MMI 3-dB couplers to form the MZI and other two MMI couplers to introduce a control light into an SOA arm. The lengths of the SOAs at the two arms were both 500 μm. The output port of the flip-flop without saturable absorbers side was connected to the upper control arm of the switch through 200-μm-long SOA to amplify the output light from the flip-flop. Since the right-lower port of the flip-flop received returning ASE noise from the MZI-SOA and amplifier, we put another SOA at the right-upper port of the flip-flop to make a balance between two lasing modes. There were five I/O port on the device: set port of the flip-flop, reset port of the flip-flop, signal port for the MZI-SOA, and two output ports from the MZI-SOA. Because of a limited number of fiber-to-waveguide coupling, we monitored only a bar output port of the MZI-SOA. Waveforms of the AOFF were monitored at the set port with a circulator.

The PIC was fabricated using same procedures as described in [7]. We used two-step MOVPE process to achieve active/passive integration. An SEM image of the fabricated device is shown in Fig. 2(b). Total chip area was 4.7×0.8 mm^2.

3. Experiments

We generated a label signal using a LD (λ = 1547.7 nm) and $LiNbO_3$ (LN) MZI modulator. Pulse width was 10 ns with repetition rate of 400 ns. The release label was delayed from the set label for 200 ns by the delay line. The payload was generated from LD (λ = 1550.9 nm) and LN modulator. The payload format was 10-Gb/s NRZ, 2^{10}-1 pseudo random bit sequence (PRBS), with 180-ns-long packet-like structures and 20-ns guard times. We also used payload signal of 40-Gb/s 2^7-1 PRBS signal at bit error rate (BER) measurements. Five channel current sources were connected to an active MMI in the AOFF, two SOAs between the AOFF and MZI-SOA, and two SOAs in the MZI-SOA, as shown in Fig. 2(a).

Figure 3 shows demonstration of all-optical packet switching using the PIC. The AOFF shows latching function of set labels as shown in Fig. 3(a) with extinction ratio of 6.2 dB. Pulse energies of set and release pulse are 10 and 15 pJ, respectively. A waveform of 10-Gb/s payloads is shown in Fig. 3(b) with 20-ns guard time. Output payloads from the device are shown in Fig. 3(c). As clearly shown, payload are successfully switched by the MZI-SOA. The output payloads have 9.5-dB contrast ratio between packets with or without set labels, so that we can note that the MZI-SOA is successfully driven by the monolithically integrated AOFF. No waveform distortion is observed with 20-ns guard time, however, pattern effects are observed due to the SOAs. Input power of the payload was +10 dBm. Conditions for five current sources were 91.3, 54, 33, 93.5, and 80.6 mA from Ch. 1 to 5, as shown in Fig. 2(a), respectively. Output light from the AOFF was monitored as the output light from the set port, extracted by a circulator. The AOFF showed a single-mode lasing with lasing wavelength of 1542.5 nm, owing to the DBRs.

Finally we measured BER curve of the 40-Gb/s, PRBS 2^7-1 payload at static switching condition. Measured BER curves are shown in Fig. 3(b) with eye patterns as the insets. We achieve error free operation with power penalty of 0.9 dB at BER of 10^{-9}. A 10-Gb/s payload is also transmitted through the PIC with 1.1-dB power penalty at BER of 10^{-9}.

From these results, we have successfully demonstrated single-chip all-optical packet switching with monolithically integrated all-optical flip-flop and switch. Both 10-Gb/s and 40-Gb/s data transmission have been demonstrated in the device, which has shown that this packet switching is transparent to the data rate. In addition, the device can drive wavelength division multiplexed (WDM) payloads since both the AOFF and MZI-SOA switch

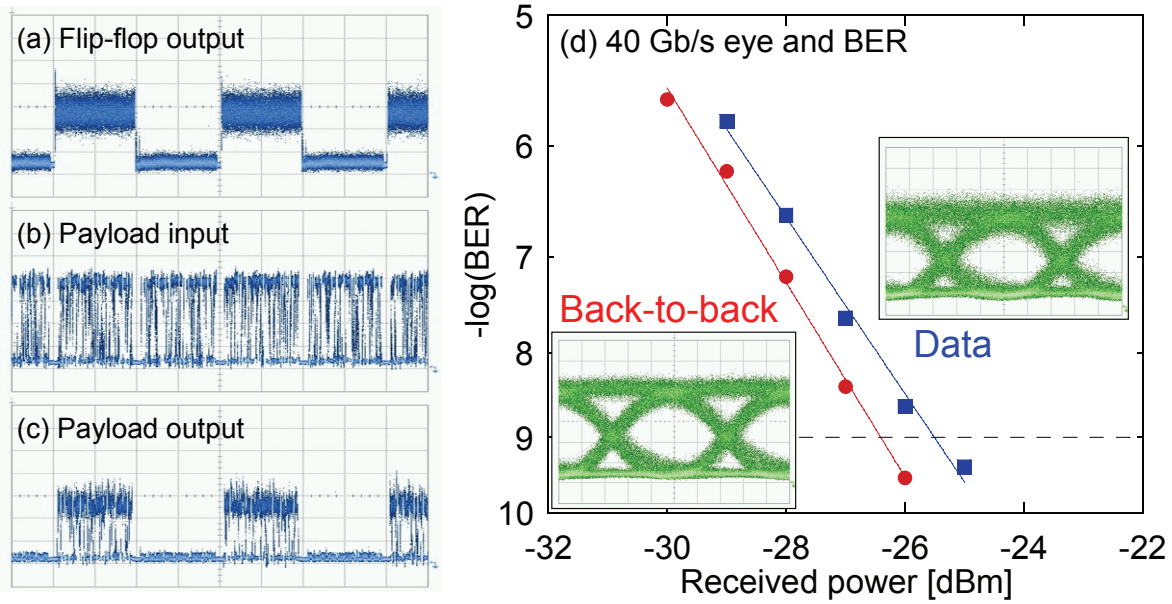

Fig. 3: Demonstration of single chip all-optical packet switching. Waveforms of (a) AOFF output, monitored at the set port, (b) input payload, and (c) output payload, respectively. Signal format was 10-Gb/s NRZ, 2^{10}-1 PRBS signal with 180-ns-long packet with 20-ns guard time. All waveforms are shown in 100-ns/div timescale. (d) BER and eye pattern of the 40-Gb/s transmitted signal at static switching condition. A power penalty of 0.9 dB is obtained at the BER of 10^{-9}. Error free operation is also demonstrated with 10-Gb/s payload.

can work if the wavelength is fit into the gain bandwidth, which is the important advantage of this scheme compared with wavelength conversions and arrayed waveguide grating routing system [9].

4. Conclusion

We have fabricated, for the first time, the PIC with monolithically integrated all-optical flip-flop (DBR-MMI-BLD) and switch (MZI-SOA) to demonstrate single-chip all-optical packet switching. The switch has been successfully controlled by the flip-flop with output packet contrast ratio of 9.5 dB. An error free operation has been achieved with both 10-Gb/s and 40 Gb/s signal with power penalty of less than 1.1 dB. This packet switching scheme is transparent to the data format. In addition, multi-color WDM optical packet can be switched with the same chip. This is the first experimental demonstration to our knowledge that the all-optical flip-flop can truly be integrated with other optical devices and work as the memory device in a photonic IC.

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