First Experimental Demonstration of Real-Time Optical OFDM Transceivers

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Abstract

Real-time optical OFDM transceivers are, for the first time, experimentally implemented, using standard commercially available components including FPGAs and DACs/ADCs. The transceivers support 1.5Gb/s transmission in directly modulated DFB laser-based 500m MMF IMDD systems.

Introduction

The concept of optical orthogonal frequency division multiplexing (OOFDM) was first proposed in 2005 [1], soon after, opportunities of employing OOFDM signals converted by directly modulated DFB lasers (DMLs) were theoretically explored over multimode fiber (MMF)-based LANs [2] and single mode fiber (SMF)-based MANs [3]. Since then, extensive investigations of OOFDM transceivers of various configurations have been reported in long-haul [4,5], MANs [6] and LANs [7]. However, all the experimental works published so far have been undertaken using non-real-time signal processing approaches, which do not consider the limitations imposed by the precision and speed of practical digital signal processing (DSP) hardware. The experimental demonstration of real-time OOFDM transceivers is critical for not only rigorously validating the OOFDM technique but also establishing a solid platform for evaluating its feasibility for practical implementation. In an optical back-to-back system, a real-time coherent OOFDM receiver has been reported recently [4], which is, however, not able to perform real-time data transmission due to the absence of a corresponding real-time transmitter.

In this paper, a real-time OOFDM transmitter and receiver based on standard commercially available components are, for the first time, demonstrated experimentally, whose transmission performance is investigated over a DML-based intensity-modulation and direct-detection (IMDD) MMF system.

Real-time OOFDM transceivers and experimental setup

Fig.1a shows the real-time experimental system configuration. The transmitter consists of an Altera Stratix II GX FPGA, which performs the real-time DSP on the data source and outputs four 8-bit samples in parallel at a rate of 500MHz. These samples are fed to an 8-bit DAC running at 2GS/s. The analog electrical signal with a 1GHz bandwidth is attenuated by a variable attenuator to adjust the modulating current injected into a 1550nm DML having a modulation bandwidth of 10GHz. The optical signal from the DML is coupled into a 500m OM1 MMF link having a 3-dB optical bandwidth of 1200MHz·km. At the receiver, a 12GHz bandwidth PIN with a TIA converts the transmitted optical signal to the electrical domain. The electrical signal is amplified by a 2.5GHz, 20dB RF amplifier and attenuated as needed to adjust the signal amplitude. The low-pass-filtered, single ended electrical signal is converted via a balun to a differential signal to feed an 8-bit ADC operating at 2GS/s, whose digital interface format is identical to the DAC input in the transmitter. Finally, the digital samples are fed to a second Altera Stratix II GX FPGA, which performs the real-time DSP on the received symbols and determines the BER. Clock synthesizers based on a common reference clock are used to generate the system clocks for the transmitter and the receiver.

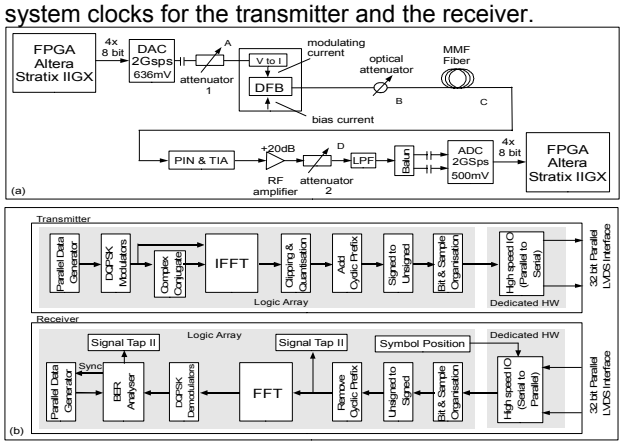

Figure 1: a) Experimental transmission system, b) Real-time OOFDM transceiver architectures

Fig.1b shows the transmitter (top) and receiver (bottom) architectures. The digital logic is entirely implemented with self-designed logic blocks. The real-time IFFT/FFT logic function is a 32 point, decimation in time, pipelined architecture, whose key parameters can be fully adjusted and optimized to minimise the finite computational error inherent in physical DSP hardware.

In the transmitter, except for the digital back-to-back case, DQPSK is considered. 32 subcarriers are used, of which 15 carry data. A 30-bit parallel data sequence feeds 15 DQPSK modulators which generate the complex data for the data-carrying subcarriers. To achieve a real-valued IFFT output, the data-carrying subcarriers are arranged to satisfy the Hermitian symmetry with respect to their complex conjugate counterparts [2]. The signed, 32

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real-valued IFFT outputs are clipped at a clipping ratio of 11.6 dB and quantized to 8 bits. A cyclic prefix of 8 samples is added to each symbol, producing 40 samples per symbol. The DAC sampling rate of 2GHz gives a symbol rate of 50MHz. The signed samples are converted to unsigned values as the DAC requires positive values only. Sample reordering and bit arrangement are performed to present the symbol data to the 32 high-speed, 10:1, serialisers in the required order and to ensure that the serialisers feed the four sample interface to the DAC in the correct sequence. In the receiver, an inverse DSP procedure, compared to that described above, is used to recover the received data, as shown in Fig.1b.

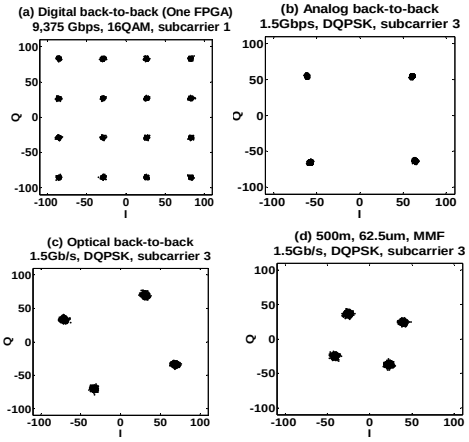

Figure 2: Subcarrier constellations for different system configurations

To achieve symbol alignment, a test symbol of a fixed pattern is sent repeatedly by the transmitter, the received symbol is detected and analyzed using the Signal Tap II, embedded logic analyzer and the Altera Quartus II software, the measured sample offset is compensated for by adding an appropriate time delay. As shown in the Fig.1b, a BER analyser block continuously detects and counts errors occurring within one million symbols. The error count is viewed via the Signal Tap II embedded analyser and an average BER is obtained over a large number of readings.

Results

To evaluate the developed real-time DSP function only, investigations are first undertaken of the performance of the digital back-to-back transmitter and receiver implemented within a single FPGA without involving the DAC/ADC. Based on a symbol rate of 156.25 MHz (less than half of the maximum FPGA clock speed), 9.375Gb/s is achieved at a BER of zero by using 16QAM. Fig.2a shows a representative constellation of subcarrier 1. This confirms the capability of the developed real-time DSP function for supporting high speed transmission.

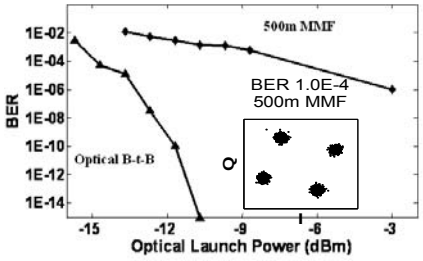

Figure 3: Measured BER performance for 1.5Gb/s transmission over a 500m MMF

By including the DAC/ADC, experimental measurements are also conducted in an analog back-to-back transmitter and receiver configuration, in which points A and D, as shown in Fig.1a, are connected with attenuator 1 being set to 3dB. With the sampling rate of 2GS/s and DQPSK, 1.5Gb/s transmission at a BER of zero is achieved with the constellation of subcarrier 3 being shown in Fig.2b. Further measurements are also performed in an optical back-to-back configuration, in which points B and C, as shown in Fig.1a, are connected. For such a case, attenuator 1, the optical attenuator and the receiver's electrical gain are taken to be 5dB, ≤6dB and 3dB, respectively, also a DFB bias current of 38mA is adopted. 1.5Gb/s transmission at a BER of $<<1.0\times10^{-9}$ is measured, as shown in Fig.3, and the constellation of subcarrier 3 is shown in Fig.2c.

Finally, experimental measurements are undertaken of 1.5Gb/s transmission over a 500m 62.5/125μm MMF IMDD link illustrated in Fig.1a. The measured BER as a function of optical launch power is plotted in Fig 3. For an optical launch power of -3dBm, a BER of $<1.0\times 10^{-6}$ is observed with a corresponding constellation of subcarrier 3 being shown in Fig.2d. The constellation of the same subcarrier for a BER of $1.0\text{x}10^{-4}$ is also inserted in Fig.3. A power penalty of 5.8dB at a BER of $1.0\text{x}10^{-3}$ is observed in Fig.3. The transmission performance is insensitive to different launch conditions.

Conclusions

The first real-time OOFDM transceivers have been implemented successfully for 1.5Gb/s transmission over a 500m MMF IMDD system. The demonstrated transceivers are potentially capable of supporting much higher data rates, when use is made of higher modulation formats and faster DAC/ADC sampling rates.

References

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