10.3Gb/s burst-mode 3R receiver incorporating full AGC optical receiver and 82.5GS/s sampling CDR for 10G-EPON systems

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Abstract *10.3Gb/s burst-mode 3R receiver incorporating full AGC optical receiver and 82.5GS/s sampling CDR for 10G-EPON is, for the first time, developed. Burst receiver sensitivity of -30.1dBm and upstream power budget of 37.6dB are successfully achieved.*

Introduction

Standardization activities of 10G-EPON (10-Gigabit Ethernet PON) systems are underway at the IEEE802.3av [1], and feasibility studies of 10G-EPON systems are intensively investigated [2]. In addition, burst-mode receivers [3,4], and burst-mode CDRs [5,6] are reported as the key technologies enabling the burst-mode upstream transmission of 10G-EPON systems. Recently, an AC-coupled burst-mode receiver has been proposed as a cost-effective solution, but it has a weakness of production margin.

In this paper, we have reported, for the first time, a "DC-coupled commercial level" 10.3Gb/s burst-mode 3R receiver incorporating a rapid AGC (Automatic Gain Control) integrated optical receiver and an 82.5GS/s over-sampling CDR to fully compliant with IEEE802.3av 10G-EPON PR30 standards. The burst receiver sensitivity of as low as -30.1dBm at the BER of 1E-3 and the upstream power budget more than 37.6dB are successfully achieved.

Configuration of burst-mode 3R receiver

Figure 1 shows the configuration of a 10G-EPON OLT burst-mode 3R receiver incorporating a burst-mode AGC optical receiver and an 82.5GS/s over-sampling burst-mode CDR. The burst-mode optical receiver consists of a burst-mode APD-preamplifier integrated AGC function, and a limiting amplifier. On the other hand, the burst-mode CDR comprises 82.5GS/s (8 x 10.3125GHz) over-sampling CDR-IC and a FPGA based data selector logical circuit. All ICs are DC-coupled. The photographs of developed burst-mode 3R receiver including a burst-mode preamplifier IC and a limiting amplifier IC, and 82.5GS/s over-sampling CDR-IC are also shown in Figure 1. The three ICs were fabricated on 0.13um SiGe BiCMOS process technology. The received 10.3Gb/s burst optical packets have different power levels and arbitrary phases, so the packet powers are normalized by amplifying each at an appropriate gain and regenerating them at the proper threshold level in a burst-mode preamplifier and a limiting amplifier, respectively. The burst-mode CDR retimes the regenerated packets from the optical burst-mode receiver, which still have arbitrary phases, to align the phases of the headers of the packets.

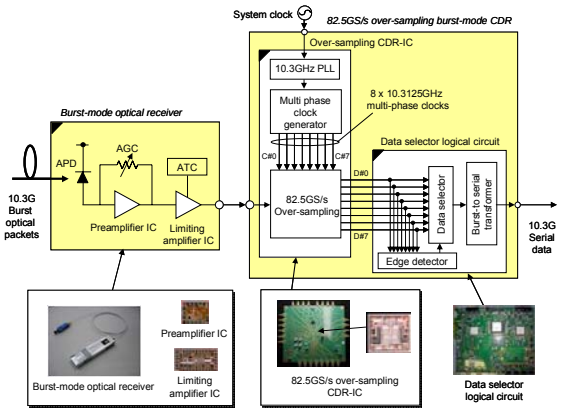

Figure1 10.3Gb/s burst-mode 3R receiver configuration

Burst-mode AGC optical receiver

The burst-mode AGC optical receiver has a small packaging of 78mm x 18.3mm x 8.5mm (XFP size), and the power consumption is less than 0.76W (+3.3V).

The burst-mode APD-preamplifier IC employs a rapid AGC function, which enables it to vary its gain continuously to compensate both the received powers and the unspecified transient responses of the ONU burst signals. The multiplication factor M of APD is set to be about eight to meet the required receiver sensitivity in IEEE802.3av standards [1]. The maximum trans-impedance gain of the APD-preamplifier of 67dBΩ and the 3dB cut-off frequency of more than 6.0GHz are obtained over the entire dynamic range. Its input-output characteristics of the APD-preamplifier IC between the temperature *Ta* of 0 and 70 degree are shown in Fig. 2, with waveforms at received powers of -26dBm, -16dBm and -6dBm. Moreover, the limiting amplifier has an ATC (Automatic Threshold Control) function, which enables it to change its threshold to

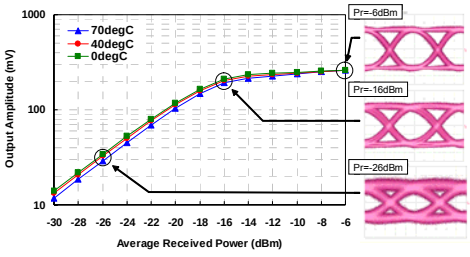

Figure2 Input-output characteristics

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the vertical center of the eye continuously.

The input (received) burst optical waveform and the output waveform from the 10.3G burst-mode optical receiver are shown in Figure 3. The input burst signal consists of first and second packets with an average power of -6dBm and –25dBm, respectively. Each packet has preamble signal (800ns) followed by PRBS31 payload data. There is no guard time between two packets for the worst condition. Figure 2 and Figure 3 show the AGC and ATC compensating a received power change continuously without reset signals. Therefore, a clear eye opening is maintained over the –30dBm to -6dBm dynamic range even with the transient response of received signal.

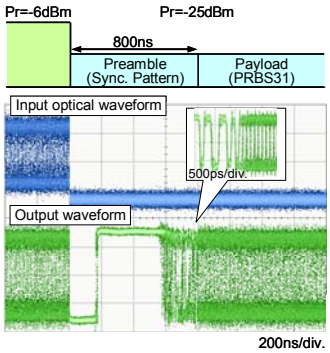

Figure3 Received burst-mode waveforms

82.5GS/s over-sampling CDR

The burst-mode CDR-IC integrates a 10.3125GHz phase locked loop (PLL), a Multi Phase Clock (MPC) generator, a data over-sampler into an 82.5GS/s over-sampling CDR-IC chip as shown in Figure 1. A data selector and a burst to series transformer are realized on an external FPGA board. The PLL and MPC generator produce eight 10.3125GHz multi phase clocks (clock #0 – clock #7) synchronized with the system clock of 161.1MHz. These eight clocks, which are clock #0 to clock #7, are sequentially shifted by 45-degrees in phase. The data sampler block can sample the incoming burst data at 82.5GS/s equivalent rate by eight 45 degrees phase-shifted clocks. The data selector detects the rising and falling edges of the data, and selects as the optimum clock with the largest phase margin that MPC whose phase is closest to the center of the detected edges. The burst packet data is then regenerated by the selected clock, and transformed into a serial data stream, which enables it to be received by a PON LSI.

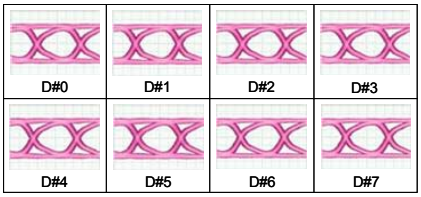

Figure4 Eight output waveforms over-sampled by multi phase clocks (C#0-C#7)

All of eight output waveform from the over-sampling CDR-IC, which are over-sampled by clock #0 – clock#7, are shown in Figure 4. All of eight output waveforms have a clear eye-opening with a low jitter peal-to-peak of less than 18ps.

BER performance of 10.3Gb/s burst 3R receiver

The BER performances of the developed burst-mode 3R receiver with 82.5GS/s over-sampling CDR are shown in Figure 5. The BER performances of the back-to-back condition and that after SMF 20km transmission are measured. The burst-mode transmitter [7] is used at ONU side, which has the wavelength of 1274nm, the output power of +7.5dBm, and the extinction ration of 6.0dB. It completely meets the IEEE802.3av PR30 standards. Figure 5 shows that a BER of 10E-3 is successfully achieved with an overload exceeding -6dBm and also at a received power as low as -30.1dBm, thus satisfying the requirements of IEEE802.3av PR30 with an appropriate margin. The burst dynamic range more than 24.1dB is achieved with the assistance of FEC RS(255, 223). The power penalty less than -0.4dB is obtained after SMF 20km transmission. Moreover, the power budget of as large as 37.6dB is successfully achieved for the burst-mode upstream transmission.

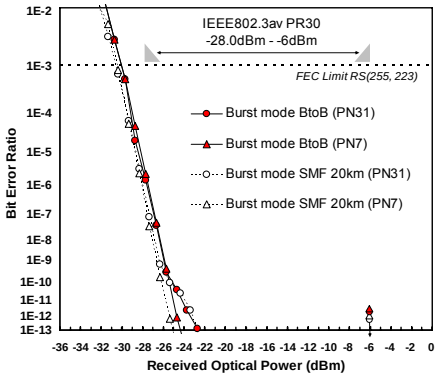

Figure5 BER performances of 10.3b/s burst-mode 3R receiver

Conclusions

In this paper, we have developed, for the first time, “DC-coupled commercial level” 10.3Gb/s burst-mode 3R receiver incorporating the rapid AGC optical receiver and the 82.5GS/s over-sampling CDR to fully compliant with IEEE802.3av 10G-EPON PR30 standards. The burst-mode 3R receiver sensitivity of -30.1dBm at the BER of 10E-3 and the upstream power budget of 37.6dB are successfully achieved.

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