All-Optical Counter Based on Optical Flip-Flop and Optical AND Gate

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Abstract An all-optical counter is presented using cascaded stages composed by SOA fiber laser based optical flip-flops and SOA four wave mixing AND logic gates. Two-bit all-optical pulse counting and optical frequency division are demonstrated.

Introduction

All-optical digital signal processing has attracted intensive research interest in recent years. By using nonlinear effects in semiconductor optical amplifier (SOA), including cross gain modulation (XGM)[1-3], four wave mixing (FWM)[3] and cross phase modulation (XPM)[4], various compact and integratable all-optical digital devices have been implemented, including optical flip-flops[1], threshold functions[1], shift registers[2], logic gates[3] and buffers[4]. In this letter, by using cascaded stages composed by SOA fiber ring laser based optical flip-flops and FWM based optical AND logic gates, an all-optical counter (AOC) is demonstrated, which can also be used as an optical frequency divider. To the best of our knowledge, this is the first time that an all-optical counter is presented. Two-bit all-optical pulse counting as well as 1/2 and 1/4 optical frequency division are demonstrated.

Operation principle

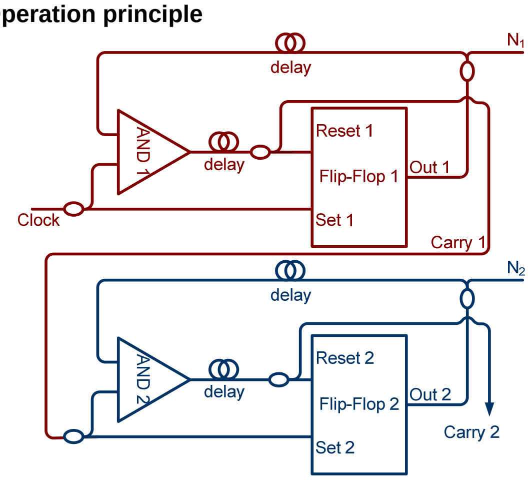

Fig. 1: All-optical counter

The proposed scheme is shown in Fig.1. The AOC is composed by two identical stages, each composed by a SOA fiber laser flip-flop and an optical AND logic gate based on FWM in SOA. Each stage has 3 ports: the input pulse, output N_i and output carry signal. Carry 1 from stage 1 is used as input of stage 2. The outputs of two flip-flops, N_2N_1, represent the output of AOC. Each flip-flop has two states, in "state 0" it outputs "0" (low optical power), and N_i=0 (i=1,2); in "state 1" it outputs "1" (high power), and N_i=1. A pulse injected into "Set i" port will set flip-flop i to "state 1"; while a pulse into "Reset i" will set it to "state 0".

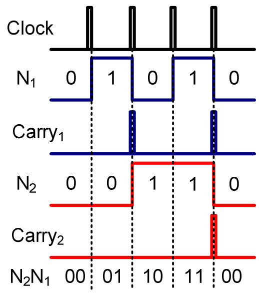

Fig. 2: Operation principle of all-optical counter

The working principle of AOC is shown in Fig.2. At first both flip-flops are in "state 0" and N_2N_1=00. When a pulse inputs, in stage 1, since N_1=0 the pulse can not pass "AND 1" and only "Set 1" receives a pulse, so flip-flop 1 is set to "state 1", and N_2N_1=01. When the second pulse inputs, it first injects into "Set 1" and flip-flop 1 remains at "state 1". Since N_1=1, the input pulse can pass "AND 1", but due to the optical fiber delay, "Reset 1" receives the pulse later than "Set 1", so flip-flop 1 is set to "state 0". The pulse from "AND 1" is used as input of stage 2 and sets flip-flop 2 to "state 1", so N_2N_1=10. When the third pulse inputs, it sets flip-flop 1 to "state 1", but it can not pass "AND 1" (N_1=0), so N_2N_1=11. Finally, when the forth pulse inputs, it passes "AND 1" (N_1=1), and since "Reset 1" receives the pulse later than "Set 1", flip-flop 1 is set to "state 0". In the same way, the pulse from "AND 1" injects into stage 2, passes "AND 2" and sets flip-flop 2 to "state 0", so N_2N_1 returns to 00. The pulse from "AND 2" can be used as the input of next stage.

Optical flip-flop and optical AND logic gate

The experimental setup of the all-optical flip-flop is depicted in Fig.3. It consists of two coupled SOA fiber ring lasers, operating at λ_1 and λ_2 respectively. In "state 1", only ring 1 is lasing and its output light is coupled into SOA 2, depleting its carriers, so ring 2 is suppressed and the flip-flop outputs "1". In "state 0", only ring 2 is lasing, while ring 1 is suppressed, so the flip-flop outputs "0". "Set" and "Reset" ports are used to change the state of flip-flop. A pulse injected into "Set" will saturate SOA 2, suppress ring 2, and then set the flip-flop to "state 1". In the same way, a pulse injected into "Reset" set the flip-flop to "state 0".

The setup of the optical AND gate is shown in Fig.4. The AND function is carried out by filtering out FWM signal ($\lambda_{FWM}=2\lambda_1-\lambda_p$) between a flip-flop output (λ_1)

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and an input pulse (λ_p). When the flip-flop is in "state 0", there is no FWM in the SOA, and the input pulse can not pass the AND gate. Variable attenuators (VOA) and a polarization controller (PC) are used to adjust the input power and the polarization state respectively, to maximize the FWM efficiency. The polarization dependence of the AND gate could be eliminated by using polarization diversity technique.

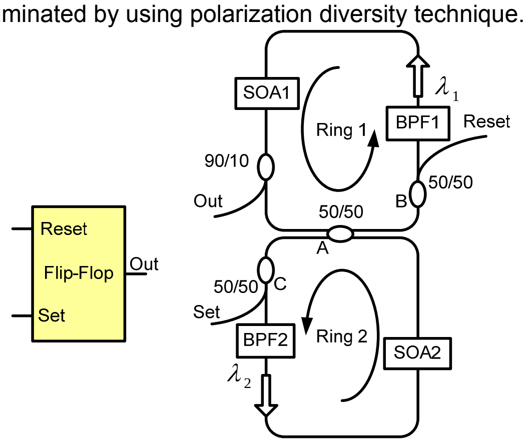

Fig. 3: All-optical flip-flop based on SOA fiber ring lasers

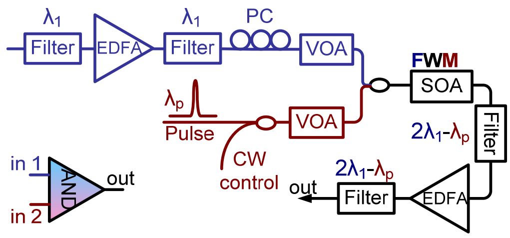

Fig. 4: All-optical AND logic gate based on FWM in SOA

Experimental results

The input clock pulse has a wavelength of λ_p=1554.1 nm, and the output of flip-flop 1 is λ_1=1552.5 nm. After FWM in "AND 1", the carry 1 signal has a wavelength of $\lambda_{c1}=2\lambda_1-\lambda_p$=1550.9 nm. The output of flip-flop 2 is λ_2=1549.3 nm, and after FWM in "AND 2", the carry 2 signal is $\lambda_{c2}=2\lambda_2-\lambda_{c1}$=1547.7 nm. All the filters we used have a 3-dB bandwidth of 0.8 nm.

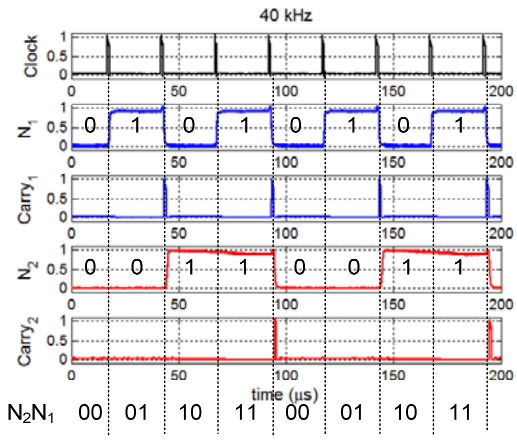

Fig. 5: Outputs of all-optical counter

In Fig.5, all-optical pulse counting is demonstrated. The input pulses have a repetition rate of 40 kHz with 1-μs pulse-width. When a pulse inputs, N_2N_1 adds 1, from 00 to 01, then to 10, 11, and finally back to 00, having a good agreement with Fig.2. In Fig.5, N_1 is a square waveform with a duty-cycle of 50% and a repetition rate of 20 kHz; N_2 is also a 50% square waveform but with a repetition rate of 10 kHz. Both carry 1 and carry 2 have the same pulse-width as the input pulse, but with repetition rates of 20 kHz and 10 kHz respectively, only 1/2 and 1/4 with respect to the input. Therefore, this scheme can also be used as an optical frequency divider.

Compared with the input pulse, it can be anticipated that both carry signals will have a CW pedestal due to the ASE noise of SOA in AND logic gates. In order to reduce these pedestals, in Fig.4, a CW light is used to saturate the SOA. It is confirmed in Fig.5 that there are no significant CW pedestals in both carry signals. In addition, Q-factor measurement is also carried out to evaluate the signal degeneration in each stage and investigate the stage cascadability. The Q-factors of N_1 and N_2 are 16.1 and 19.9 respectively, only depending on the properties of flip-flops. The Q-factor of input pulse is 32.5. Due to the low repetition rate and gain-tilt mechanism of EDFA, carry 1 has a Q-factor of 17.0. By exploiting the aforementioned CW light to saturate the SOA, we are able to obtain carry 2 with a Q-factor of 15.0, only slightly lower than carry 1, further confirming the cascadability of this scheme.

The pulse counting rate of this scheme is mainly limited by the state switching time of optical flip-flops, which is due to the discrete device implementation of flip-flops. In our case, the cavity length of fiber lasers in flip-flops is 40 m, corresponding to ~1 μs switching time. Photonic integration can reduce the switching time lower than 100 ps by shortening the cavity length to millimetres and make GHz counting possible[5].

Conclusions

For the first time as we know, an all-optical pulse counter is demonstrated. By cascading identical stages composed by a SOA fiber laser flip-flop and an optical AND logic gate, we present an optical counter, which can also be used as an optical frequency divider. Two-bit optical pulse counting is implemented, as well as 1/2 and 1/4 optical frequency division. Q-factor measurements confirm the feasibility of the proposed solution and the cascadability of single stage in order to increase the maximum bit-number of counting. Finally, photonic integration of optical flip-flops would allow the courting speed beyond GHz.

References

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