A 82.5-GSample/s (10.3125-GHz x 8 phase-shifted clocks) sampling IC for 10G-EPON burst-mode CDR

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Abstract *New very high-speed 82.5-GS/s sampling IC and its incorporated burst-mode CDR compliant for 10G-EPON is presented. The 82.5-GS/s sampling CDR successfully achieved a high pulse-width distortion tolerance of +/- 0.53 UI under distorted burst packets received condition of BER=10^{-3}.*

Introduction

10G-EPON (10-Gigabit Ethernet PON) systems hold great promise for the coming generation of access networks. Standard and related research activities for such high bandwidth 10-Gbps based EPON are being energetically pursued [1,2]. A 10-Gbps based burst-mode CDR (clock and data recovery) is one of the most important PMD (physical medium dependent) devices for implementing the 10G-EPON system and several 10-Gbps based burst-mode CDR techniques have been proposed [3,4].

Over-sampling technique based burst-mode CDR is a promising candidate for the 10G-EPON CDR, and a quick burst-mode data recovery of the first bit by a 10.3 GHz x quad-rate sampling CDR has been reported in [4]. However, there still remain technical challenges to meet 10G-EPON syetem requirement. The 10G-EPON demands the very severe power budget of 30 dB (PR30 class) with FEC (forward error collection) [1], and it needs that the PMD layer link can operate at a high jitter accumulated condition of more than BER=10^{-3}, as RS(255,223) FEC input condition. Especially for the burst-mode CDR, a pulse-width distortion tolerance [5], which represents a margin to the worst case of the jitter accumulation, is most critical parameter for the CDR design. To our knowledge, however, a burst-mode CDR satisfied with the 10G-EPON required pulse-width distortion tolerance has not been reported yet.

In this paper, we present new high-speed sampling IC of over 82.5 GS/s sampling rate for the 10G-EPON burst-mode CDR. Due to the obtained high-speed sampling resolution, we have successfully achieved a 10G-EPON compliant burst-mode CDR with a high pulse-width distortion tolerance of +/- 0.53 UI under a large jitter accumulated condition of BER=10^{-3}.

82.5-GS/s sampling IC and burst-mode CDR

Figure 1 shows the block diagram of our 82.5-GS/s sampling IC and the whole configuration of a 82.5-GS/s burst-mode sampling CDR. The sampling IC integrates two main function blocks: a 10.3 GHz x 8-phase PLL and a 82.5 GS/s sampler circuit. The 8-phase PLL can generate 10.3-GHz x 8 phase-shifted clocks, #0 to #7, which are sequentially shifted by 45-degrees (1/8) in phase. These clocks are synchronized with the system clock at 161.1 MHz. The sampler circuit can sample the incoming burst data at over 82.5 GS/s equivalent rate via the 10.3 GHz x 8 phase-shifted clocks. Thus, the input burst-data is converted to 8 sets of 1/8 phase-shifted and rapidly system synchronized data D#0 to D#7, which are sampled by clock #0 to #7 respectively. The sampling IC composes the CDR with a FPGA based data selector logic circuit. In the logic circuits, a data edge detector finds rising and falling edges from the sampled data D#0 to D#7. A data phase decider judges the optimum recovery phase from the edge phase detected result, based on our data-phase decision-algorithm [4,5]. Finally, a data selector circuit selects the data sampled by the clock of the recovery phase selected by the phase decider, and outputs the selected data as the optimum CDR recovered data.

Figure 2 shows photographs of the sampling IC (chip-on-board). We employed a high *ft* = 200 GHz 0.13 um SiGe BiCMOS for the sampling IC, in order to achieve the over 82.5 GS/s sampling rate. The IC chip size is as small as 3.5 mm x 3.3 mm.

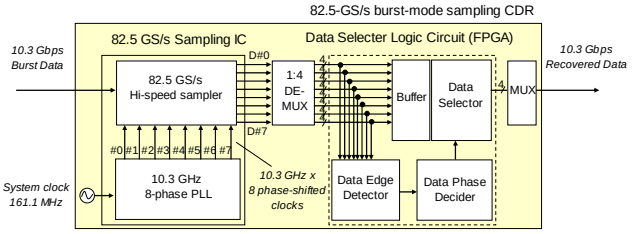

Figure 1: Block diagram of 82.5-GS/s sampling IC and CDR

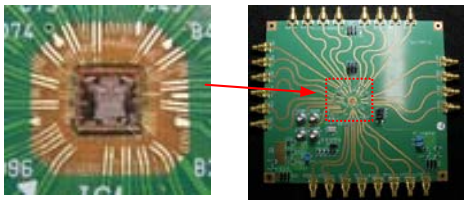

Figure 2: Photographs of the 82.5-GS/s sampling IC (COB)

Performance of the 82.5-GS/s sampling CDR

Firstly, we have evaluated a sampling resolution of the 82.5-GS/s sampling IC. Figure 3 shows the measured results of output BERs of the sampled data D#0 to D#7 at the sampling IC output, when the relative delay between the input data and the sampling clocks of #0 to #7 was varied from 0.0 UI

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(unit interval) to 1.5 UI. The test data pattern was 10.3 Gbps PRBS2^{31}-1. From the result, it can be clearly seen that the error free region of each sampled data output BER of D#0 to D#7 was sequentially shifted by 1/8 phase (12 ps) of 10.3 Gbps data. Thus, incoming data was successfully captured by the sampling IC at the sampling resolution of a high 12 ps, which equal to 82.5 GHz (10.3 GHz x 8) equivalent rate.

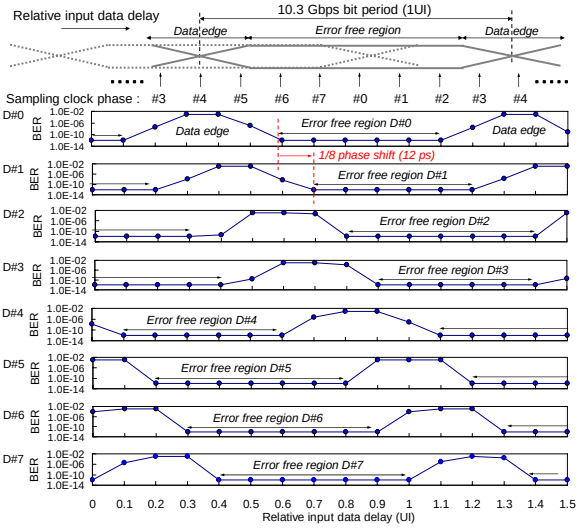

Figure 3: Measured result of the sampling resolution

This obtained very hi-speed sampling resolution can elevate a pulse-width distortion tolerance of the over-sampling based CDR [5], because it can sample very narrow eye-opening region of data. Figure 4 shows the test setup of the burst-mode pulse-width distortion tolerance test. In the experiment, we used our 1.27 um burst-mode transmitter [6] and burst-mode receiver consisted of a APD-TIA (transimpedance amplifier) and a 2R with differential output. A pulse-width distortion generator was inserted at the input side of the sampling CDR in order to add any pulse-width distortion onto the optical receiver output data without degradation of the received sensitivity. The pulse-width distortion was added by adjusting DC offset between the (+) and the (-) signals of the differential line. Figure 5 shows the measured eye waveforms of CDR inputs and recovered data. In the test, the added pulse-width distortion of +/-0.53 UI is corresponded to the worst *Dj* (deterministic jitter) of the 10G-EPON system jitter requirement [1]. The pulse-width distortion degree was adjusted at small *Rj* (random jitter) region of less than BER=10^{-12}. As shown in the Fig.5, it is found that the sampling CDR can recover clear data from distorted input data added +/- 0.53 UI pulse-width distortion plus large receiver output jitter of BER=10^{-3}. The jitter peak of the recovered data was as low as 18 ps. Figure 6 shows results of the burst-mode pulse-width distortion tolerance test. The burst-mode waveforms at the pulse-width distortion of +0.53UI and BER=10^{-3} input condition are also shown in the figure. We measured the power penalty of the minimum received sensitivity at BER=10^{-3} when the pulse-width distortion was varied from -0.68 UI to +0.68 UI. Burst packets used for the test had 800 ns of overhead (OH) [1] followed by 300 us of PRBS2^{31}-1 payload data. The packets included 300 us dark period time. It is seen in Fig.6 that a pulse-width distortion induced penalty is as low as 0.1 dB within the required pulse-width distortion region of +/- 0.53 UI, due to the high-speed sampling rate of 82.5 GS/s. And also, a quick and stable burst response time of less than 800 ns at BER=10^{-3}, which including the transmitter and receiver burst response time, was successfully achieved. Thus, our 82.5-GS/s sampling CDR suits it to act as a burst-mode CDR for 10G-EPON systems.

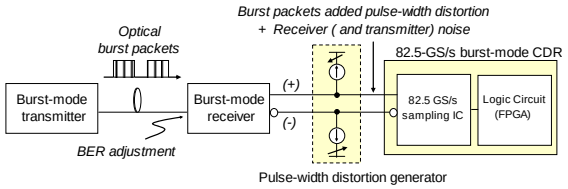

Figure 4: Experimental setup of the burst-mode pulse-width distortion tolerance test

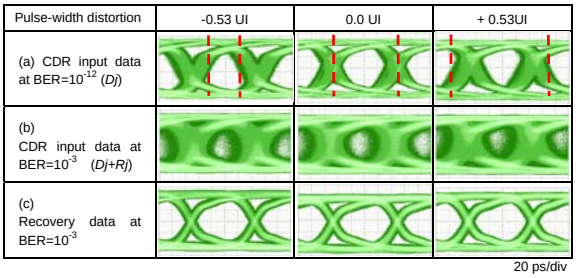

Figure 5: 82.5-GS/s CDR input and output eye-waveforms

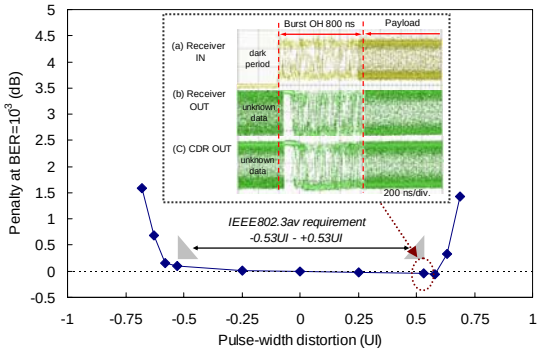

Figure 6: Measured result of the burst-mode pulse-width distortion tolerance test at BER=10^{-3}

Conclusions

A 82.5-GS/s sampling IC and its incorporated 10G-EPON compliant burst-mode CDR was demonstrated. Due to the very high sampling rate of 82.5 GS/s (1/8 phase x 10.3 Gbps), a high burst-mode pulse-width distortion tolerance of +/-0.53 UI under a large jitter condition of BER=10^{-3} was successfully achieved.

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