25 Gbps EML TOSA Employing Novel Impedance-Matched FPC Design

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Abstract *25 Gbps EML TOSA employing novel impedance-matched flexible printed circuit design realizes 30 GHz 3-dB bandwidth and a low-jitter optical waveform with 39 % mask margin for 100 Gbps Ethernet applications.*

Introduction

Standardization of 100 Gbps Ethernet (100GbE) is now being discussed, where four-wavelength 25 Gbps non-return to zero (NRZ) optical lanes are adopted [1]. The most plausible solution for transmitter side is the combination of four electro-absorption modulated laser (EML) transmitter optical sub-assemblies (TOSAs) with 4ch-WDM coupler. Previously, a temperature tolerant 25 Gbps EML chip with high dynamic extinction ratio [2] and a 25 Gbps EML module with low dispersion penalty [3] have been reported. However, for practical use of EML in 100GbE transponder, the connection between an EML TOSA and a printed circuit board (PCB) with little signal deterioration up to 25 Gbps is required. Flexibile printed circuit (FPC) as electrical interface is one of the solutions for cost-effective and compact design, which has been widely used for 10 Gbps EML TOSA or XMD-MSA [4]. However, the high electrical reflection due to the impedance mismatch at the connection point between the PCB and the FPC deteriorates over 10 Gbps data signal transmission.

In this paper, we demonstrate 25 Gbps EML TOSA with FPC electrical interface employing novel impedance-matched design, which enables low-reflection connection between the FPC and the PCB and low-jitter 25 Gbps optical waveforms.

TOSA structure

Fig. 1 shows a photograph of the TOSA. Package size excluding fiber-pigtail part is 5.2 mm x 5.8 mm x 9.45 mm. FPC is attached on the electrical-feed pads of the package.

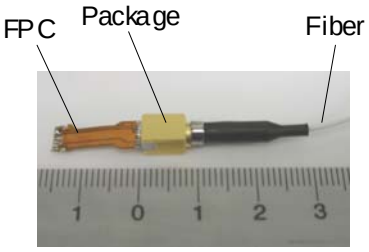


Fig. 1 Appearance of the EML TOSA

In order to realize a low-jitter waveform at high speed data rate, it is important to suppress the electrical reflection at the interfaces between different transmission lines. A crucial interface is the connection point between the PCB and the FPC, where large impedance mismatch occurs. We propose novel impedance-matched FPC connection design for the superior 25 Gbps signal transmission.

Design

Fig. 2(a) is the schematic drawing of the connection point between the PCB and the FPC. Both the PCB and the FPC have microstrip transmission lines. At the connection point, GSG (ground-signal-ground) pads are formed on both edges to connect RF signal. Here signal via hole in Fig. 2(a) can be modelled as inductance. Also, signal-line part with no GND layer in the FPC (indicated as line w/o GND in Fig. 2(a)) can be modelled as an inductance as shown in equivalent circuit in Fig. 2(a). Therefore, electrical reflection due to the impedance mismatch occurs in high frequency region. In Fig. 3, the curve (a) is the simulated electrical reflection S_{11} at the interface between the PCB and the FPC and the corresponding 25 Gbps simulated optical waveform is shown. Jitter in the waveform increases due to the high electrical reflection.

To solve this problem, we propose a novel connection design shown in Fig. 2(b). We add GND pads near the FPC signal line, which are connected to the GND layer in the PCB through GND via holes. These GND pads and the FPC signal line form capacitance, which can compensate the extra inductance or optimize electrical reflection. The simulated electrical reflection S_{11} at the interface between the PCB and the FPC in the proposed design is show as the curve (b) in Fig. 3, along with the corresponding 25 Gbps simulated optical waveform. Additional GND pads well suppress the electrical reflection below -20 dB from DC to 25 GHz, which results in low-jitter 25 Gbps optical waveform.

978-3-8007-3173-2

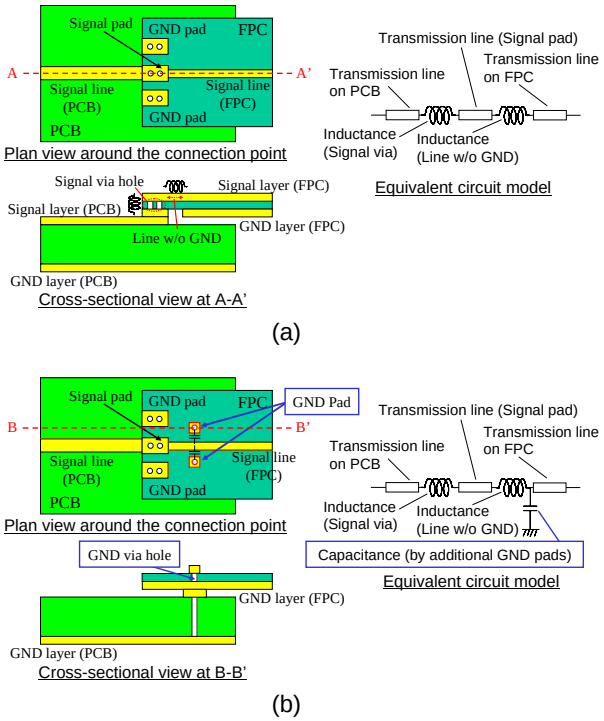


Fig. 2 Schematic drawing of the connection point in (a) conventional and (b) proposed design

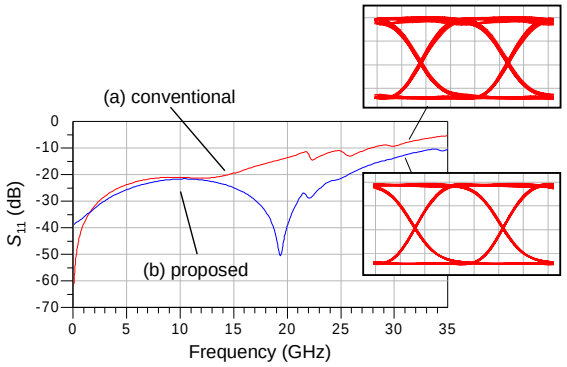


Fig. 3 Simulation results of electrical reflection S_{11} and 25 Gbps optical waveforms with conventional and proposed FPC connection design

Experiment

The EO response S_{21} of the fabricated TOSA employing the proposed design is shown in Fig. 4. The 3-dB bandwidth of S_{21} was as large as 30 GHz. Fig.5 (a) is the optical waveform of this TOSA. The laser-chip temperature was set at 40 degrees C and laser was biased by 80 mA. The TOSA was modulated by NRZ 25.78125 Gbps PRBS31 (2^{31}-1 pseudo random bit sequence) with 2.0 Vpp amplitude and 0.25 V offset bias. The optical modulation amplitude and extinction ratio were 2.8 dBm and 7.1 dB, respectively. The wavelength was 1309 nm, which complies with 100GbE specification.

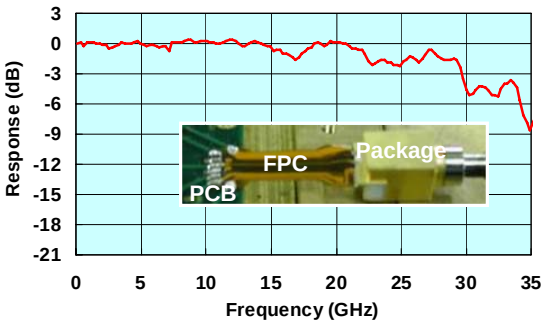
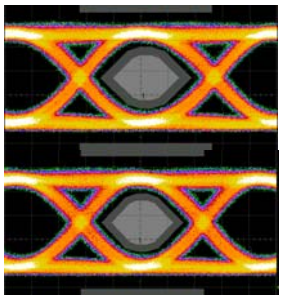


Fig. 4 Measured EO response S_{21} of the TOSA (Inset : TOSA connected to the board)



(a) (b)

Fig. 5 Optical waveform with 4th bessel filter at (a) 25.8 Gbps (b) 28 Gbps (*1000 waveforms integration*)

A low-jitter optical waveform with 39 % mask margin was realized.

Furthermore, we evaluated the optical waveform at 28 Gbps for the future FEC (forward error correction) extension (Fig. 5(b)). Even at the higher bit rate of 28 Gbps, a low-jitter optical waveform with 33 % mask margin was demonstrated.

Finally, we measured the thermo-electric cooler power consumption of the TOSA. Low-power consumption of less than 0.6 W at the TOSA case temperature between -5 and 80 degrees C was confirmed.

Conclusions

A compact and cost-effective 25 Gbps EML TOSA with FPC electrical interface was demonstrated employing novel impedance-matched FPC design for the low-reflection electrical connection to the PCB. 3-dB bandwidth up to 30 GHz and low-jitter 25.8 / 28 Gbps optical waveforms with 39 / 33 % mask margin were realized. We believe that this newly developed EML TOSA is promising for 100GbE application.

References

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