Demonstration of a Lossless Monolithic 16x16 QW SOA Switch

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Abstract *10Gb/s error-free operation of the first monolithic 16x16 quantum well semiconductor optical amplifier switch is demonstrated. The switch has a 2dB facet-to-facet gain and a minimum power penalty of 2.5dB.*

Introduction

In recent years, the demand for optical networks able to rapidly re-route signals between moderate numbers of input and output fibres has encouraged research into the use of photonics in switching. As optical switches using MEMs technology and the like have limited speed[1], semiconductor optical amplifier (SOA) based photonic switches have attracted growing interest owing to their ability to achieve lossless switching of high capacity data with nanosecond switching timescales[2]. Such switches have recently undergone much development, with integrated 2x2[3], 4x4[4] and 8x8 port switches[5] being reported, the latter being achieved with multiple integrated 1x8 switching elements. Scaling further requires unprecedented levels of component integration[6].

However, for practical applications, devices with port counts of at least 16x16 are needed for systems applications[7]. Recently, feasibility studies have shown that 16x16 port counts can be achieved using cascaded 4x4 devices with fibre interconnections[8].

In this work we report the first monolithically integrated 16x16 port SOA based optical switch, incorporating ~1100 individual components. The switch is re-arrangably non-blocking and has a chip area of 40mm[2].

Device details

The monolithic integrated 16x16 switch used for this work is based on a 3-stage hybrid Clos-Tree structure, shown in figure 1. Three columns of four 4x4 port switching elements are connected by two shuffle networks to create the 16x16 port switch. Each of the 4x4 switching elements comprises its own input and output shuffle networks and 16 SOA gates.

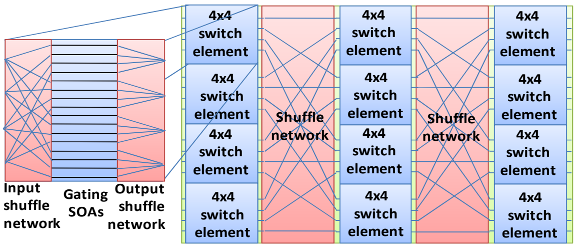

Fig. 1: Schematic of 3-stage 16×16 switch architecture based on 4×4 switch elements

The switch is fabricated from all active material with a 6 QW AlGaInAs active region, grown on an InP substrate. The paths through the switch are constructed from 2µm ridge waveguides, whereas the SOA gates are tapered to 4µm wide ridges. The waveguide interconnections comprising the shuffle networks are constructed from deep etched total internal reflection (TIR) mirrors and beam splitters formed with tapered waveguides.

The waveguides in each shuffle network are biased to provide a small loss between successive SOA gates, to minimize the buildup of amplified spontaneous emission. The SOA gates provide routeing functionality and sufficient gain to allow lossless operation of the entire switch.

It should be stressed that the current chip is re-growth free i.e. without active-passive interfaces. It is believed that the inclusion of, for example, passive shuffle networks would reduce ASE, nonlinear distortion and power consumption.

Figure 2 shows the layout of the switch. Each path has three gating SOAs and goes through eight shuffle sections with a mean path length of 9mm. The switch contains 192 SOAs, 210 waveguide crossings, 288 splitters, 424 etched corner mirrors and has dimensions of 6.3mm x 6.5mm.

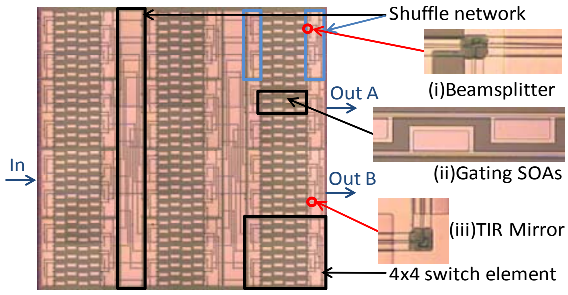

Fig. 2: Schematic of the 16x16 switch showing the 4x4 switch elements and shuffle network sections (left). Insets show (i) waveguide beam splitter, (ii) gating SOA waveguides and (iii) TIR turning mirror.

Experimental details

The integrated switch is mounted on a thermo-electric cooler and operated at 15°C, with lensed fibres used to couple light on and off the chip. Operation of the entire 16x16 switch requires 192 high bandwidth electrical connections for the gating SOAs and 26 low speed connections for the shuffle. We switch between two outputs so that the dynamic performance of the device may be characterized.

The switch is operated with selected gating SOAs driven switched between 0 and 100mA. This ensures good crosstalk performance within the switch. The shuffle networks associated with the first two banks of switching elements are each biased at 495mA, while the shuffle network for the last bank is biased at 600mA. The two large intermediate shuffle networks are each biased at 700mA. This drive current is equivalent to 750mA per path.

Optical measurements are performed using a tunable laser and optical spectrum analyser to determine the c.w. performance of the switch, with fibre coupling losses estimated from photocurrent measurements. Dynamic optical measurements are performed using a 10Gb/s 2^{31}-1 PRBS signal from a Mach-Zehnder modulator and an optically pre-amplified and filtered receiver.

Results

The switch has a facet-to-facet gain of 2dB at 1557.5nm with fibre coupling losses measured to be 4dB per facet. The TIR mirror loss has been measured to be 4dB. Optimisation of the design is expected to improve this to 2dB per mirror[9]. The 3dB on-chip output saturation power is -6.3dBm with a 3dB spectral bandwidth of 9nm. The switch output has an in-band optical signal-to-noise ratio (OSNR) of 15.5 dB. As can be seen from figure 3, the switch operates with a power penalty of 2.5dB at a BER of 10^{-9} for an on-chip input power of -15dBm. An input power dynamic range (IPDR) of >4dB is measured for a power penalty of less than 4dB, as can be seen in figure 4.

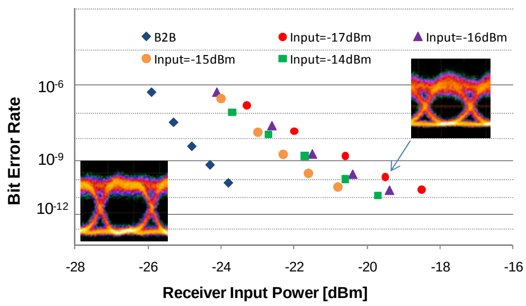

Fig. 3 Bit error rates and eye diagrams showing low power penalty for a number of different input powers

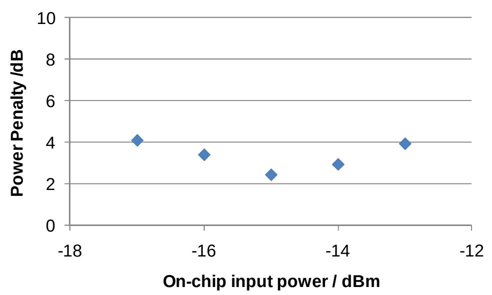

Fig. 4 Power penalty as a function of on-chip input power

Dynamic switch performance is assessed by modulating the drive current to the gating SOAs. The dynamic operation of the switch is demonstrated by switching packets between two paths (the output from one path being shown in figure 5). This is achieved by switching on/off the middle gate SOAs from 0mA to 100mA with a 1ns electrical transition. A 15dB optical extinction ratio is observed at the output when the switch is operated, as the final gate SOAs and shuffle networks remain on and therefore contribute to ASE at the output. The non-optimised switching times are measured to be 10ns and 3ns for the rising and falling edges, respectively.

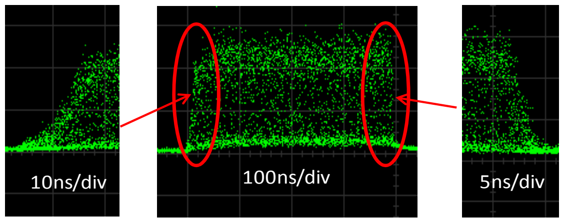

Fig. 5 Switching of 10Gb/s signal with 10ns rise-time and 3ns fall-time.

Discussion

The power consumption of the current chip is estimated to be ~12W for a fully non-blocking 16x16 interconnection, a power density of 0.3W/mm^2 which is a relatively modest value for heat dissipation. This power consumption could be reduced further by the replacement of the current active shuffle networks with their passive equivalents. Currently the shuffle networks consume ~60% of the drive current and so this approach may reduce the power requirement to <5W (or 300 mW/path).

Conclusions

The first monolithically integrated 16x16 SOA crosspoint switch is demonstrated. The switch has a positive facet-to-facet gain, and an output saturation power of -7dBm. Routing of a 10Gb/s signal is achieved with a minimum power penalty of 2.5dB, showing its promising ability for high speed switching applications such as packet switching.

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