BiNMOS: A Basic Cell for BiCMOS Sea-of-Gates

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Abstract

A basic cell (BiNMOS) for BiCMOS sea-of-gates is described which achieves twice the performance with area comparable to a popular CMOS sea-of-gates. The cell, which also efficiently implements SRAM, was designed with a statistics driven methodology to determine the number and sizes of each device type.

Introduction

CMOS sea-of-gates (or channel-less gate arrays) combine the integration level required to implement integrated subsystems (e.g. microprocessors, signal processors, peripheral controllers) with the fast turn-around and low development cost of conventional gate arrays. When compared to custom implementations, however, sea-of-gate implementations suffer from reduced performance mainly due to: (i) longer interconnect length, and (ii) routing over diffusion. Another drawback of CMOS sea-of-gates is the inefficiency (or inability) to implement RAM, which is commonly used in large applications.

To enhance the performance of CMOS gate arrays the use of BiCMOS technology has been suggested [1]. Several BiCMOS gate arrays (and sea-of-gates) have been reported [2, 3, 5]. Several [3, 5] employ two bipolar devices in every internal cell for use in the totem-pole BiCMOS buffer configuration. This can be wasteful in area since the capacitive loading on most internal nets in a typical gate array design is low enough that the bipolar devices are not needed. In [2] a ring of BiCMOS cells surrounding a core of pure CMOS sea-of-gates array is employed. This approach overcomes (to some extent) the problem of low utilization of bipolar devices, but at the expense of awkward placement and routing for the highly loaded internal nets. CMOS sea-of-gates cells have been reported that implement the 6-transistor CMOS SRAM cell [4]. Their drawback, however, has been that the small devices needed for the SRAM cell are wasted when the cell is used for implementing logic.

BiNMOS Cell

In this paper we describe a BiCMOS sea-of-gates basic cell (BiNMOS cell) which, for the same design rules, achieves comparable area per "gate" as existing CMOS sea-of-gates with potentially twice the performance. The BiNMOS cell is also capable of implementing a single SRAM cell (single or dual port). The topology of the BiNMOS cell is depicted in Fig. 1. It comprises two sections, a compute section consisting of 4 small N and 4 small P devices, and a drive section consisting of a single bipolar device and 2 large N devices.

A statistics driven (RISC-like) methodology was employed in the design of the BiNMOS cell. The number and sizes of each device type (P, N, Bipolar) were determined based on (i) typical net capacitive loading distributions, (ii) statistics of macro usage in typical designs, (iii) the requirements for implementing the 6-transistor SRAM cell, and (iv) single layer (metal 1) internal macro routability.

The decision to employ a single bipolar device in each cell was arrived at as follows. Circuit simulation was used to obtain the delay vs. capacitive loading characteristics (Fig. 2) for two inverters. The first is a CMOS inverter with device sizes typical of sea-of-gate cells [2] and the second is a totem-pole BiCMOS inverter. Examination of Fig. 2 revealed that the pull-down time for the N device is shorter than or comparable to that of the BiCMOS inverter up to about 0.4 pF. Given typical net capacitive loading distributions of the type depicted in Fig. 3, we see that more than 60% of the nets do not require a bipolar pull-down. On the other hand, the pull-up time of the P device is worse than that of the BiCMOS inverter even for low capacitive loading. Therefore a bipolar pull-up alone can greatly improve performance, whereas a bipolar pull-down is only needed for a small fraction of the nets.

These observations naturally led to the BiNMOS inverter shown in Fig. 4, which provides performance comparable to that of the BiCMOS inverter over most of the

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capacitive loading range of interest, but requires less area. The BiNMOS inverter also has the advantage of pulling down to ground with no threshold voltage drop.

Performance

The drive section of the BiNMOS cell was chosen to implement the output section of the BiNMOS inverter. Two large N devices were employed: (i) to achieve performance comparable to BiCMOS for over 90% of all nets, and (ii) to facilitate the implementation of the SRAM cell. The delay vs. capacitive loading of the BiNMOS inverter is plotted in Fig. 4, for one (BiNMOS1) and two (BiNMOS2) parallel N devices. Assuming that BiNMOS1 inverters are used up to 0.4 pF and BiNMOS2 are used thereafter, the average delay weighted by the reciprocal distribution of Fig. 3 is 0.65 ns, compared to 1.43 ns for the CMOS inverter (approximately a factor of two). For the lognormal distribution the BiNMOS delay was 0.64ns and the CMOS was 1.36ns. The same (or a more favorable) ratio should hold true for other gates since, while all BiNMOS gates share the same drive stage, CMOS gates will have series transistors in either the pull-up or pull-down networks.

Area Efficiency

The choice of 4 small N and 4 small P devices in the compute section of the BiNMOS cell was made so that the most frequently used macros (2 and 3 input gates, D-latch, 2 input MUX) can each be implemented in a single cell.

The area efficiency of the BiNMOS cell was evaluated as follows. First, the BiNMOS cell was layed out in TI's 0.8μ BiCMOS technology (Fig. 5). Next, the average number of cells per macro, as weighted by two sets of macro usage statistics, was computed for the BiNMOS cell as well as for the widely used 4-transistor CMOS cell [2]. Based on the layout in Fig. 5 the area of the BiNMOS cell was estimated to be 0.5 that of the CMOS cell (W/L the same as the BiNMOS large N device), when layed out in the same technology. This factor was used to compare the normalized average area per macro for the two cells. Using statistic set 1 (Table 1) we found that the BiNMOS average area/macro was 1.20 compared to 1.46 for the CMOS cell. For statistic set 2 the BiNMOS area was 1.43 and the CMOS area was 1.42. We concluded that designs implemented with the BiNMOS cell require approximately the same area as those implemented in an all-CMOS sea-of-gates. We believe that the area consumed by a BiNMOS design would be even less if the effect of the efficiency of implementing SRAM blocks and the fact that fewer dedicated buffering cells are required were taken into account.

Test Chip

A BiNMOS test chip has been designed and fabricated in TI's 0.8μ BiCMOS technology. The test chip consists of a 4 X 22 array of BiNMOS cells. The test structures include a ring oscillator, a 4 bit SRAM core, 5 types of buffers, a MUX, and a shift register. Ring oscillator measurements indicate a basic BiNMOS inverter delay of 240ps (FO=1), a result which agrees well with simulation.

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References

[1] A. R. Alvarez and D. W. Schucker, "Bi-CMOS Technology for Semi-Custom Integrated Circuits," *Proc. IEEE Custom Integrated Circuits Conference*, 1988, pp. 22.1.1–22.1.5.

[2] Anthony Wong, et. al., "A High Density BiCMOS Direct Drive Array," *Proc. IEEE Custom Integrated Circuits Conference*, 1988, pp. 20.6.1–20.6.3.

[3] L. Lin, D. Rosky, H. Truong, "A 9100 Gate ECL/TTL Compatible BiCMOS Gate Array," *Proc. IEEE Custom Integrated Circuits Conference*, 1987, pp. 190–194.

[4] H. Takahashi et. al., "A 240K Transistor CMOS Array with Flexible Allocation of Memory and Channels," *IEEE Journal of Solid State Circuits*, vol. SC-20, no. 5, pp. 1012–1017, Oct. 1985.

[5] H. Nakashiba et. al., "A Subnanosecond BiCMOS Gate Array Family," *Proc. IEEE Custom Integrated Circuits Conference*, 1986, pp. 63–66.

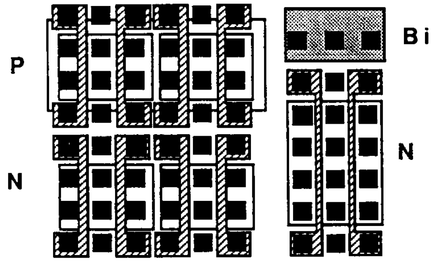
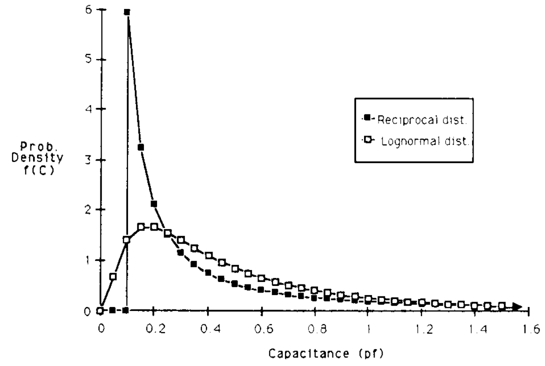


Fig. 1: BiNMOS Basic Cell



Reciprocal Distribution: $f(C) = g/C^{\gamma}$ mean=0.6 γ=1.5

Lognormal Distribution: $f(C) = \frac{1}{(\sqrt{2\pi})\sigma C} \exp(-(\ln(C) - \mu)^2/2\sigma^2)$

mean=0.6 variance=.468

Fig. 3: Net Capacitance Distribution

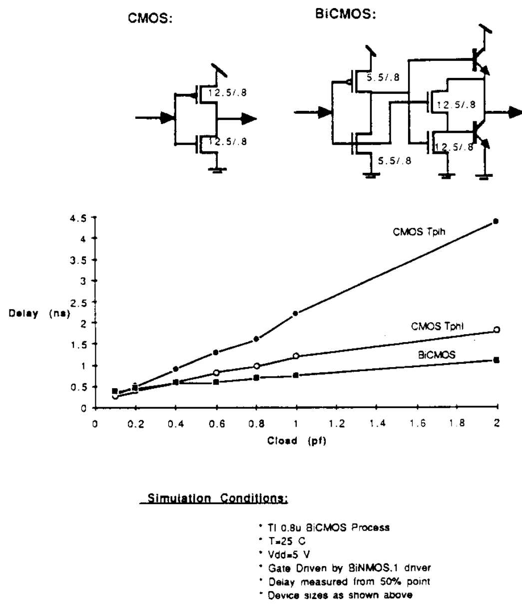


Fig. 2: CMOS vs. BiCMOS Delay

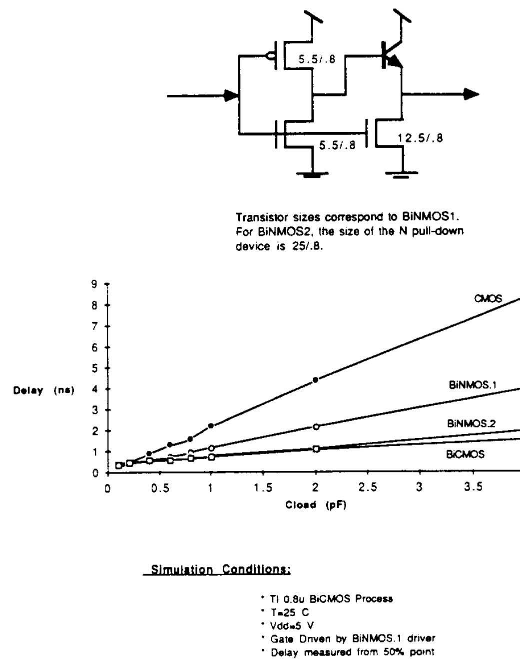


Fig. 4: BiNMOS Delay vs. Cload

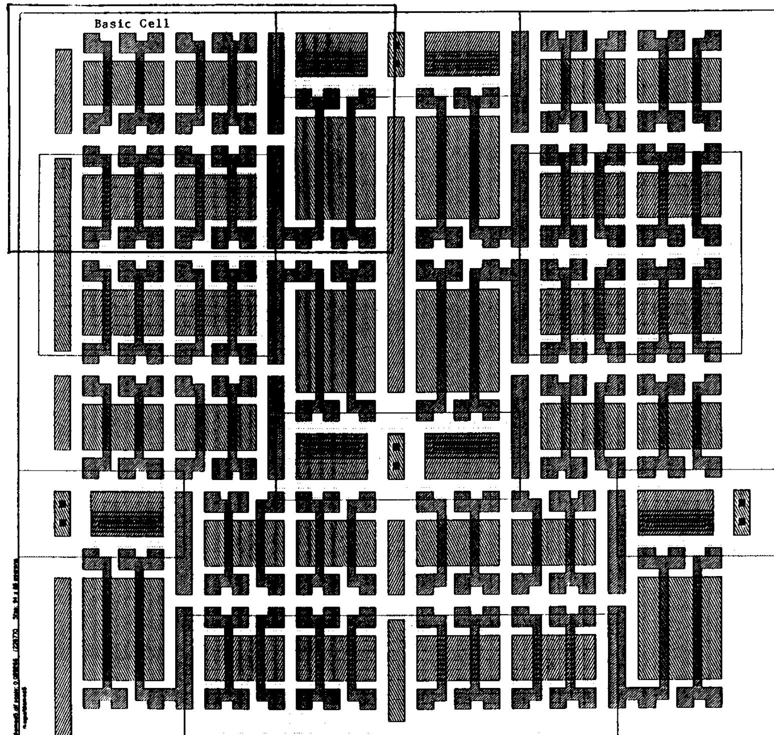


Fig. 5: BiNMOS Cell Layout and Tiling

Table 1

Macro Usage Statistics -- Industrial Source 1
(21 chips, 51000 Macros)

Macro Name	No. of 4-T cells	No. of BiNMOS	Fraction Used
2W AND/OR/NAND/NOR	2	1	0.324567
SRL	9	3	0.10208
Inverter	1	1	0.100949
Buffer	2	0	0.084517
2W XOR/NXOR	3	1	0.062609
3-4 W AO/AOI	3	2	0.054499
3W NAND/NOR/AND	3	1	0.035280
4-6 W AO/AOI	4	3	0.029160
2:1 MUX	3	1	0.027367
4W AND/OR	3	2	0.017368
Gtd D Latch(hp)	5	2	0.014697
1 W S/R SRL(hp)	12	3	0.010136
5-6W AND/OR	4	2	0.009064
D Flip Flop(hp)	8	2	0.008499
4W NAND(hp)	4	2	0.008109
L2 * SRL	12	4	0.007154
5-8 W OA	5	4	0.006179
5-6W NAND(hp)	5	2	0.005672
2:1 MUX(hp)	4	1	0.005575
2W XOR(hp)	4	1	0.004074
7-8W AND	5	3	0.003957
3-4 W OAI(hp)	3	3	0.003957
5-8 W OA(hp)	5	3	0.003372
Avg Cells/Macro:	2.91267	1.20475	
Normalized Area:	1.45634	1.20475	

(4-T Cell uses 20% more area)

hp= high power version of gate
SRL=LSSD shift register latch

Macro Usage Statistics -- Industrial Source 2
(6 chips, 17600 Macros)

Macro Name	No. of 4-T cells	No. of BiNMOS	Fraction Used
2W NAND/NOR	1	1	0.1078860
2W AO/AOI	2	2	0.1038029
Inverter	1	1	0.0882704
2W AND/OR	2	1	0.0527808
D FF w/scan	9	4	0.0409320
2:1 MUX	3	1	0.0400249
3W NAND	2	1	0.0378139
Gtd. D Latch	4	1	0.0346391
2W XOR/NXOR	3	1	0.0312943
4W NAND/NOR	2	2	0.0264753
Gtd. D latch w/C	4	2	0.0298203
inv to 3 inv	2	1	0.0167243
3-state buf(hp)	4	2	0.0166109
DFF S/scan/hp	10	4	0.0164408
Gtd. D latch(hp)	5	1	0.0162141
Inverter(hp)	2	1	0.0160440
DFF w/scan(hp)	9	3	0.0155905
DFF	6	2	0.0147968
3-state buf	3	2	0.0136062
4:1 MUX (hp)	7	3	0.0117921
full adder	9	4	0.0117921
4:1 MUX	6	3	0.0111117
Others	4.86	1.976	0.0944498
Avg Cells/Macro:	2.83973	1.43075	
Normalized Area:	1.41986	1.43075	

(4-T Cell uses 1% less area)