Digital Pixel Image Sensors

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1. Introduction

CMOS image sensors have received much attention over the last decade, offering the promise of ultra low power and camera-on-chip integration in standard fabrication processes. This year over 30 million such sensors have been shipped with estimated annual growth rate of over 40%. Most CMOS image sensors shipped today are application-specific (e.g., optical mouse) or used in low-end applications (e.g., PC-cameras, toys). They are fabricated in older CMOS technologies (0.35μm and above) and as a result have very limited integration. With few exceptions [1], these sensors have significantly lower performance than CCDs.

Recent work on modifying submicron CMOS processes to enhance their imaging performance [2] will enable dramatic increase in imaging system integration, which can be used to reduce power consumption and cost. We argue that integration can also be used to improve sensor performance beyond CCDs and to enable new imaging applications. In particular we show that the recently developed Digital Pixel Sensor (DPS) architecture integrated with memory and signal processing circuits on the same chip can achieve significantly higher dynamic range than CCDs and enable new applications ranging from image blur prevention to accurate optical flow estimation and its applications.

2. DPS Architecture

The DPS architecture employs an ADC per pixel and digital data is read out of the image sensor array in a manner similar to digital memory. DPS offers several advantages over analog image sensors, such as, Passive and Active Pixel Sensors [3,4], including better scaling with CMOS technology due to reduced analog circuit performance demands and the elimination of read-related column fixed-pattern noise (FPN) and temporal noise. More significantly, by employing an ADC and memory at each pixel, massively parallel A/D conversion and digital readout provide unlimited potential for high-speed ``snap-shot'' digital imaging. The main disadvantage of DPS is its large pixel size relative to conventional analog image sensors due to the inclusion of more transistors in each pixel. This disadvantage disappears as technology scales to 0.18μm and below since DPS pixel size scales well with technology, quickly approaching the practical lower bound set by imaging optics and dynamic range considerations.

Our group has developed three generations of DPS implementations. The first DPS comprised an array of 128×128 pixels with a sigma-delta ADC shared within each group of 2×2 pixels and was implemented in 0.8μm CMOS technology [5]. The sigma-delta technique can be implemented using simple circuits and is thus well suited to pixel-level implementation in advanced processes. However, since decimation is performed outside the pixel array, too much data needs to be read out of the array. The second generation of DPS solves this problem by using a Nyquist rate ADC approach [6]. The sensor comprised an array of 640×512 pixels with a multi-channel bit serial (MCBS) ADC shared within each group of 2×2 pixels and was implemented in 0.35μm CMOS technology. Implementing MCBS ADC only requires a 1-bit comparator and a 1-bit latch per each group of 4 pixels. The control signals needed to perform the A/D conversion are shared by all ADC's resulting in low pixel FPN. Other important features of this sensor include its support for auto-zeroing to reduce offset FPN and electrical testability of all circuits (except photodiodes) that greatly simplifies its testing and characterization. The sensor achieved 16 bits of dynamic range using the multiple capture technique.

Our latest DPS chip [7] was the first image sensor to be implemented in a 0.18μm CMOS technology and the first to achieve a continuous throughput of 10,000 frames/s or 1 Gpixel/s. It comprised an array of 352×288 pixels each containing a photogate circuit, a 1-bit comparator, and 8 3T memory cells in an area of 9.4μm×9.4μm. Bit-parallel single slope A/D conversion is performed simultaneously for all pixels via globally distributed analog ramp and gray coded digital signals generated outside the array. When a comparator switches, the gray coded value at the time of switching is stored in the pixel-level memory.

3. High Frame Rate Applications

The high frame rate operation of DPS enables the implementation of many still and video rate image processing applications. The idea is to use the high frame rate to oversample the scene and thus obtain more accurate information about its illumination and motion.

This information can then be used to: (i) enhance image quality, e.g., by extending dynamic range or preventing image blur [9], (ii) obtain accurate optical flow estimates [10] that can be used as basis for several video processing applications, or (iii) simplify many basic vision algorithms, e.g., feature tracking.

The first application we demonstrated using DPS is high dynamic range imaging using multiple capture [6]. Several techniques have been proposed for extending sensor dynamic range. Only multiple capture, however, has been shown to extend dynamic range at the low illumination end. In [12], an algorithm for synthesizing a high dynamic range, motion blur free, still image from multiple image captures is presented. The algorithm consists of two main procedures, photocurrent estimation to reduce read noise [10] and motion/saturation detection to extend dynamic range at high illumination and to prevent image blur [9]. Another application we developed uses a high frame rate video sequence to obtain accurate optical flow estimates at standard video rate. This method was recently used to develop the first viable method for correcting sensor gain FPN [13].

To explore these applications, we designed and prototyped an experimental PC-based high speed CMOS imaging system around our latest DPS chip [12]. The system comprises a PCB that houses the DPS chip, provides the analog and digital signals needed to operate it, and interfaces to a PC via three 20MHz 32-bit National Instrument I/O cards. Front end optics is provided by attaching a metal box with a standard C-mount lens to the PCB. The system is software programmable through MATLAB.

Such multi-chip system, however, is not suited to commercial applications. In [8], we argued that by integrating DRAM and signal processing circuits with the sensor, which becomes feasible at 0.18μm technology, these high frame rate applications can be implemented at low cost and power consumption.

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