Techniques for Pixel Level Analog to Digital Conversion

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ABSTRACT

Two techniques for performing pixel level analog to digital conversion (ADC) are reviewed. The first is an oversampling technique which uses a one bit first order $\Sigma\Delta$ modulator for each 2×2 block of pixels to directly convert photocharge to bits. Each modulator is implemented using 17 transistors. The second technique is a Nyquist rate multi-channel-bit-serial (MCBS) ADC. The technique uses successive comparisons to convert the pixel voltage to bits. Results obtained from implementations of these ADC techniques are presented. The techniques are compared based on size, charge handling capacity, FPN, noise sensitivity, data throughput, quantization, memory/processing, and power dissipation requirements for both visible and IR imagers. From the comparison it appears that the $\Sigma\Delta$ ADC is better suited to IR imagers, while the MCBS ADC is better suited to imagers in the visible range.

Keywords: Pixel Level ADC Sigma Delta MCBS

1. INTRODUCTION

Both visible and infrared (IR) image sensors frequently use CMOS readout circuitry. Examples include visible CMOS active pixel sensors (APS),[1] PtSi IR sensors, and HgCdTe IR sensors.[2] The readout circuitry can either be integrated with the photodetectors, e.g. CMOS APS and PtSi sensors, or bonded below the photodetectors, e.g. HgCdTe sensors. The function of most readout circuitry today is to transfer the signals from the pixels to the output of the chip. However, as technology scales, other functions such as ADC, dynamic range enhancement, offset and gain FPN correction, storage, and signal processing, can be integrated with the readout. Such integration should help improve performance, and reduce system cost, and power.

In this paper we are concerned with ADC integration. ADC may be performed at at the chip level using a single high speed ADC, at the column level using multiple lower speed ADCs, or at the pixel level using very low speed ADCs. Pixel level ADC has many advantages over chip and column level ADCs. These include low noise, low power dissipation, and the ability to continuously observe the pixel outputs. Pixel level ADC helps reduce system noise by confining all of the analog circuits and signals to the pixel and only transmitting digital data. Continuous observation of the pixel allows for oversampling to reduce noise, extend dynamic range, and increase the charge handling capacity of the pixel.

Although pixel level ADC has many advantages, conventional ADC architectures are not easily implemented at the pixel due to limited area. Few attempts have been made to implement pixel level ADC.[3-8] Most authors[3-5] have focused on voltage-to-frequency (VF) conversion at each pixel so that no analog signals need to be transferred. However, since the ADC is performed one row at a time, this technique is essentially a column ADC technique rather than a true fully parallel pixel level ADC. The first true pixel level ADC, described by Fowler et al,[6,7] uses an oversampling technique. Each pixel employs a one bit $\Sigma\Delta$ modulator implemented with very simple and robust circuits. The $\Sigma\Delta$ modulators all operate simultaneously. The first Nyquist rate pixel level ADC is described by Yang et al.[8] The ADC is a multi-channel-bit serial (MCBS) quantizer. Each pixel employs a one bit comparator and a latch and is also implement using very simple circuits.

In this paper we review these recently developed techniques and compare them based on size, charge handling capacity, FPN, noise sensitivity, data throughput, quantization, memory/processing, and power dissipation. The comparison suggests that the $\Sigma\Delta$ ADC is better suited to IR imagers, while the MCBS ADC is better suited to imagers in the visible range.

The remainder of the paper is organized as follows: first we describe the architecture of a pixel level ADC readout circuit. We then present the circuits for the two pixel level ADC techniques and report measured results from sensor implementations. Finally we compare the two ADCs and discuss their applicability to visible and IR sensors.

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2. ARCHITECTURE

Although pixel level ADC has many advantages over column and chip level ADC, its implementation is seriously constrained by limited pixel size. This precludes the use of bit–parallel ADC techniques, such as single slope, since they require at least m–bits of memory per ADC to implement m–bit conversion. Moreover, conventional bit-serial techniques such as successive approximation or algorithmic ADC require complex circuits and very precise and matched analog components. As a result, they are also not suited to pixel level implementation. To overcome the pixel area limitation we developed two bit serial ADCs. The first is based on an oversampling technique[6] and the second is based on a Nyquist rate technique.[8]

Both techniques use the same overall readout architecture as shown in Figure 1. The readout circuitry consists of an $N \times M$ array of pixel blocks, a row decoder, a sense amplifier for each column, and a column decoder/output multiplexer. Each pixel block consists of an ADC connected to one or more photodetectors. Through out the remainder of this paper we assume an architecture where each ADC is shared among a 2×2 block of pixels. The readout circuitry operates in the same way as a read only memory using the row and column decoders and simple sense amplifiers. Each pixel block generates one bit at a time, which results in a two dimensional array of bits, i.e. "bit plane" (see Figure 2). Each video frame, thus, consists of L bit planes. Note that this data format is very different from the typical raster scan format. An important advantage of this architecture is that the speed of the analog circuitry is constant, independent of the array size. The bit plane output format is also beneficial for progressive data read out.

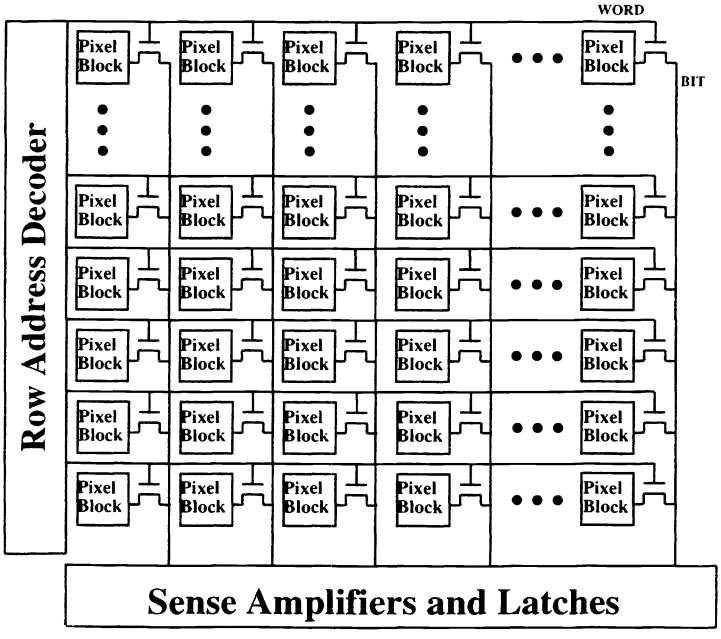

Figure 1. Block Diagram of an Image Sensor with Pixel Level ADC

Figure 3 shows a first order one-bit $\Sigma\Delta$ modulator.[9] It consists of an integrator and a one bit quantizer. The $\Sigma\Delta$ modulator generates data at L times the Nyquist rate. The oversampled data is decimated to the Nyquist rate using a digital low pass filter. The resulting SNR of the Nyquist rate data can be computed as

$$\text{SNR} = 9\log_2 L - 5.2\text{dB}. \tag{1}$$

The main disadvantage of this ADC technique is that the output data rate before decimation is much larger than the equivalent Nyquist rate ADC. If decimation is to be performed off chip, this poses severe requirements on the I/O bandwidth, especially for high speed or large format sensors.

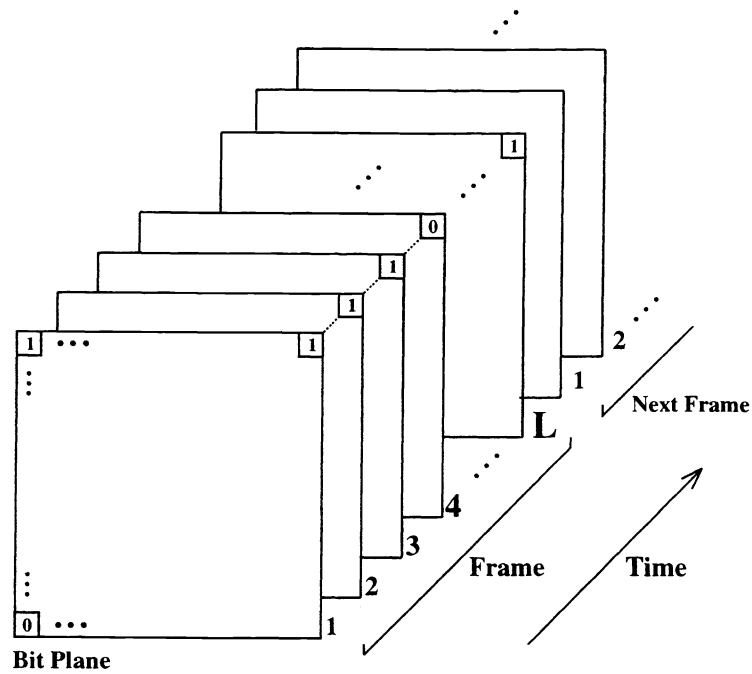

Figure 2. Bit planes generated by pixel level ADC

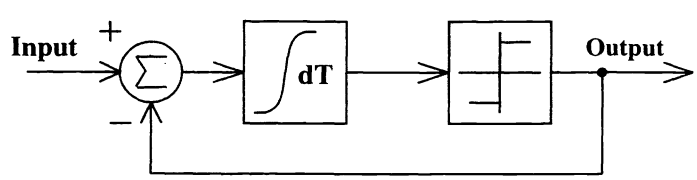

Figure 3. $\Sigma\Delta$ Modulator.

To reduce data rate, we developed the Nyquist rate MCBS ADC technique.[8] A block diagram of the MCBS ADC is shown in Figure 4. It consists of both pixel level and chip level circuitry. The pixel level circuitry consists of a one bit comparator and a latch. The chip level circuitry consist of a simple state-machine and an m-bit DAC. The state-machine produces **BITX** and the input to the DAC necessary to generate the **RAMP** signal.

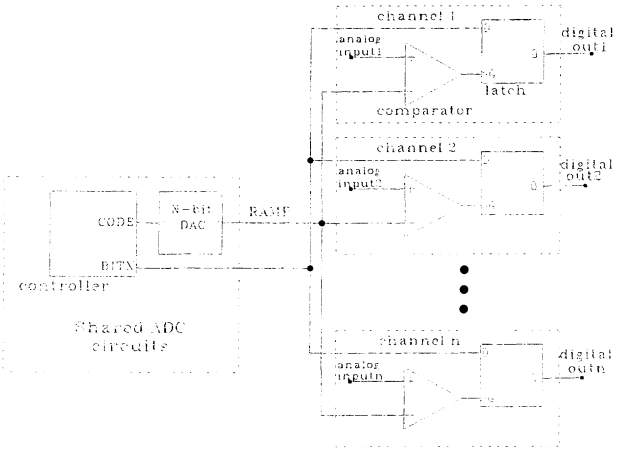

Figure 4. MCBS ADC Block Diagram.

The MCBS ADC performs quantization by successive comparisons between the analog pixel signals and **RAMP**. The result of each comparison is stored in the latch using **BITX** and then read out one bit plane at a time. The operation of the MCBS is decribed in detail by Yang.[8] We provide the following one bit example to illustrate the operation of **RAMP** and **BITX**. Assuming that the input range of the ADC is (0,1], a one bit conversion can be performed by setting **BITX** to 0 and stepping **RAMP** from 0 to $\frac{1}{2}$. If the analog input is less than $\frac{1}{2}$ then 0 is latched, otherwise **BITX** is switched to 1 after **RAMP** has transitioned, and the output of the latch is 1.

The fundamental speed/resolution limit on the MCBS ADC is limited by comparator design. As discussed by Yang et al,[8] to perform m–bit quantization at least $2^m - 1$ comparisons must be performed. Also, assuming uniform quantization, the gain of the comparator must be proportional to 2^m. Therefore, the gain bandwidth product of the comparator must exceed the product of the frame rate, $2F_d$, the number of comparisons, and the minimum required gain.

3. CIRCUITS

In this section the circuits for the two pixel level ADCs are presented. In discussing the circuits we assume that photodiodes are used and that each ADC is shared by a 2×2 pixel block. The array is read out one quarter bit plane at a time.

3.1. ΣΔ Modulator

A circuit schematic of the multiplexed pixel level ΣΔ modulator is given in Figure 5. The circuit uses 17 transistors, and consists of a clocked comparator, a one bit DAC, and a 4:1 analog multiplexer. The ADC operates as follows. The pixels are selected one at a time using the select signals **S0, S1, S2,** and **S3**. Figure 6 shows the control signal waveforms when pixel D0 is selected. ΣΔ modulation is performed on the photocharge integrated by the photodiode junction capacitance. The junction voltage of the selected photodiode is quantized using a comparator with regenerative feedback clocked via **CK**. The comparator is biased to operate in subthreshold in order to reduce power and noise, increase gain, and reduce any leakage current in the D/A converter. The bias current is set to the minimum value needed to achieve the desired sampling rate.[10] The quantized value is converted to charge using a 1 bit D/A converter and fedback to the photodiode. The 1-bit D/A is implemented using an analog shift register

similar to a 3-phase CCD transfer structure. If the output of the comparator **FEEDBACK** is low, a sequence of 3 control pulses **DUMP, STORE, CK** (as shown in Figure 6), dump a fixed amount of charge on the photodiode junction capacitance. The total charge, q_d, transferred to the photodiode junction capacitance is

$$q_d = (V_{dd} - V_{STORE} - V_{tp})C_{ox}W_{16}L_{16}, \tag{2}$$

where V_{dd} is the power supply voltage, V_{STORE} is the low voltage on **STORE**, C_{ox} is the oxide capacitance of M16, W_{16} is the width of M16, and L_{16} is the length of M16. Note that equation 2 is only valid for $V_{dd} - V_{STORE} - V_{tp} > 0$. As shown in equation 2 the voltage of **STORE** can be used to control the amount of charge transferred to the photodiode junction capacitance. Therefore, electronic shuttering can be performed by adjusting **STORE**'s voltage. At the completion of each clock cycle a single bit is generated and read out using the bit line **BIT**.

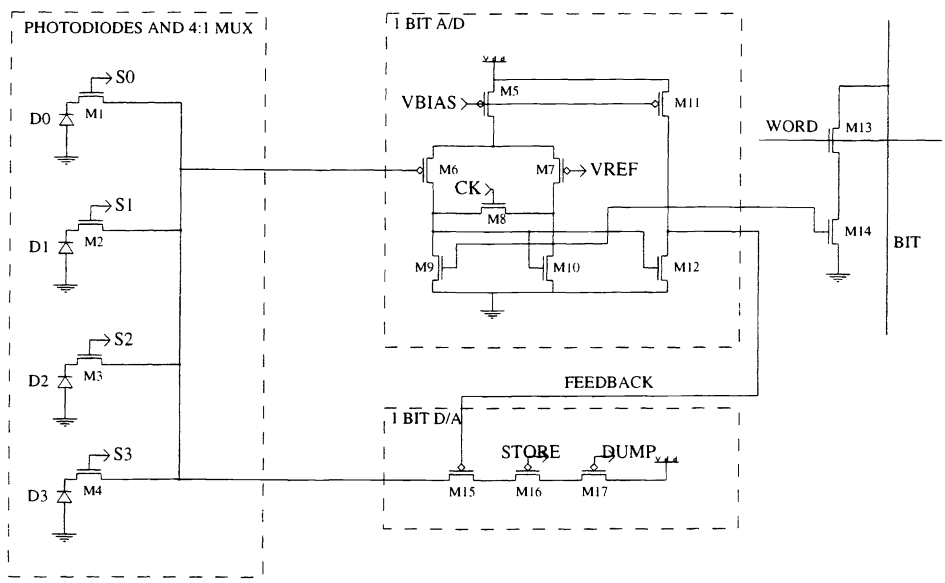

Figure 5. $\Sigma\Delta$ Modulator Circuit Schematic

The main advantages of this circuit are small size, low sensitivity to transistor noise, no offset FPN, and large charge handling capacity. Input referred noise caused by reseting the one bit DAC, and 1/f and thermal noise from the comparator are very small in comparison to the quantization noise and therefore can be neglected for most applications. Moreover, the DAC noise is reduced by integration, and the comparator noise is reduced by feedback. The offset FPN of the $\Sigma\Delta$ modulator is zero due to the first order differencing of all noise and offset errors in the loop as shown by Candy.[9] The large charge handling capacity is due to the feedback charge from the 1 bit DAC. For example, if the oversampling ratio is 64, the charge handling capacity of this circuit is about 64 times larger than an APS with the same size photodiode.

The main shortcomings of this circuit include gain fixed pattern noise (FPN), poor low light response, nonlinear response, charge mixing between multiplexed pixels, and high output data rate. The gain FPN is caused by variations in M16 parameters from modulator to modulator. The poor low light response is due to the fact that for a $\Sigma\Delta$ modulator, the quantization interval associated with the lowest input signal range has the lowest resolution. The nonlinear response is due to the nonlinear charge to voltage characteristics of junction photodiodes. This effect can be reduced to acceptable levels by increasing the reverse bias voltage or by reducing the voltage swing across the photodiode. Charge mixing between pixels is caused by charge sharing between the gate of M6 and the selected photodiode. Moreover, when **S0** is selected some charge is transfered to the gate of M6, and when **S0** is not selected and **S1** is selected the residual charge on the gate of M6 is mixed with the charge on D1. Oversampling causes the

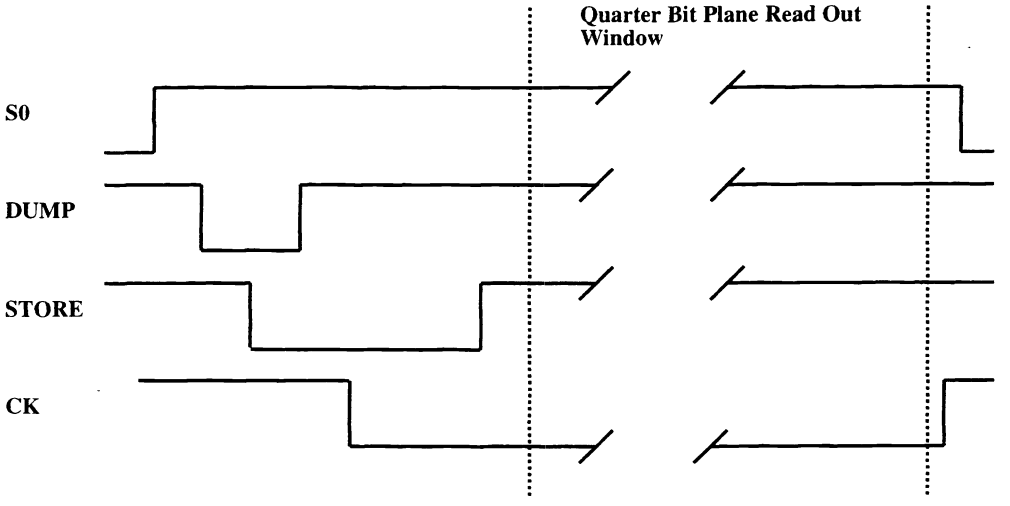

Figure 6. $\Sigma\Delta$ Modulator Control Signal Waveforms.

output data rate to be at least

$$\frac{2^{\frac{6}{9}(m+\frac{5.2}{6})}}{m} \tag{3}$$

times higher than an m-bit Nyquist rate ADC.

3.2. MCBS ADC

A schematic of the multiplexed pixel level MCBS ADC circuit is shown in Figure 7. The circuit uses 18 transistors, and consists of a comparator, a one bit latch, and a 4:1 analog multiplexer. The ADC operates as follows. The pixel voltages are converted into digital values one at a time. Each conversion starts by sampling a pixel voltage through the analog multiplexer, using **S0, S1, S2,** or **S3**, to the gate capacitance of M5. The resulting voltage on the gate of M5, V5, is

$$\mathrm{V5} = V_{reset} - \frac{V_{photo} C_d}{C_d + C_{gs5}}, \tag{4}$$

where V_{reset} is the reset voltage of the photodiode, V_{photo} is the photon induced photodiode voltage, C_d is the junction capacitance of the diode, and C_{gs5} is the gate capacitance of M5. This assumes that the voltage on the gate of M5 is greater than its threshold voltage and that the junction capacitance C_d is approximately linear. **RAMP** is applied to the positive input of the comparator. The comparator consists of a transconductance amplifier followed by a Wilson current mirror and a cascode output load. It is biased to operate in subthreshold to maximize gain and minimize power. **BITX** is used as the input to the latch, and is the result of the comparison between the analog input and **RAMP**. When the comparator changes state the last value of **BITX** is stored in the latch. The latch operates as a 2T DRAM cell where M1 is the write port pass transistor and M2 is the read port buffer. After each **RAMP** sequence one bit is read out from the latch. If an m-bit conversion is performed then the latch must be read m different times. After the pixel voltage has been converted into a digital value the pixel is reset by turning on M4 and the appropriate photodiode select device. This allows the comparator to operate as a opamp with unity gain feedback, and therefore the voltage on **RAMP** plus the offset voltage of the comparator is stored on the selected photodiode. This removes most of the comparator offset. Note that this reset feature also allows complete testability of the ADC.

The main advantages of this circuit include, small size, low gain and offset FPN, and complete testability. Gain FPN is minimized by sharing the circuits that generate the global signals **RAMP** and **BITX**. Offset FPN is due

to comparator offset and switching feedthrough of M4. Autozeroing is used to remove the comparator offset, and switching feedthrough is reduced by using M5. The residual photodiode referred offset error charge, q_{error}, is

$$q_{error} = (-\frac{V_{offset} + V_{reset}}{1 + A_v} + \frac{V_{dd}C_{ov4}}{C_d + C_{gs5} + C_{ov4}} + \frac{\alpha C_{ox4}W_4L_4(V_{reset} - V_{tp4})}{C_d + C_{gs5}})(C_d + C_{gs5}), \quad (5)$$

where V_{offset} is the offset voltage of the comparator, A_v is the open loop gain of the comparator, α is the proportion of M4's channel charge that is transferred to the gate of M5, C_{ov4} is the overlap capacitance between the gate and source of M4, W_4 is the width of M4, L_4 is the length of M4, and V_{tp4} is the threshold voltage of M4. Complete testability is achieved by using the reset mode, where an arbitrary voltage can be stored on the photodiode using **RAMP**. This voltage can then be digitized and used to characterize the ADC.

The main shortcomings of this circuit include moderate comparator gain–bandwidth, and reduced photodetector sensitivity caused by the sample and hold capacitor M5. The moderate comparator gain–bandwidth is caused by limited area. The maximum resolution of the ADC is determined by the gain of the comparator, and the speed of the ADC is determined by both the gain and the bandwidth of the comparator. Assuming subthreshold operation[11] and that the early voltage and gate efficiency of all the transistors are the same, it can be shown that the gain of the comparator is approximately

$$A_v = \frac{1}{6}\left(\frac{V_{early}\kappa}{\frac{KT}{q}}\right)^2, \quad (6)$$

where V_{early} is the early voltage of the transistors, κ is the gate efficiency of the transistors, and $\frac{KT}{q}$ is the thermal voltage. Again using the same assumptions, it can be shown that the gain bandwidth of the comparator is approximately

$$\text{GBW} = \frac{I_{bias}\kappa}{8\pi\frac{KT}{q}C_{output}}, \quad (7)$$

where I_{bias} is the tail current of the differential pair, and C_{output} is the output capacitance of the comparator. The gain of the comparator is controlled by the length of the transistors and the gain bandwidth is controlled by the tail current. A typical voltage gain for this comparator in a 0.35μm process at room temperature is 2000–4000 with a gain bandwidth of 5–20MHz. This translates into an ADC resolution of up to 11 bits. The reduced photodetector sensitivity is due to charge sharing between the photodiode capacitance and the sample and hold capacitor M5. Equation 4 shows that the photon induced voltage on a photodiode is attenuated by a factor of $\frac{C_d}{C_d+C_{gs5}}$ when it is sampling onto the gate capacitance of M5.

4. RESULTS

In this section results are presented for both $\Sigma\Delta$[7] and MCBS ADC[8] implementations. Table 4 shows the process and sensor characteristics for both implementations.

Figure 8 shows the measured output from a single $\Sigma\Delta$ modulator as a function of time. To reconstruct the digitized pixel value a decimation filter[9] is used. This is performed externally in software. For example, the lower graph in Figure 8 shows 3 "ones" in 8 clock cycles; if we use a counter as a simple decimation filter, the pixel output is 3/8 of the maximum output value.

The $\Sigma\Delta$ ADC achieves a shuttered dynamic range* greater than 83dB. This is the case since the magnitude of the feedback D/A converter can be varied by a factor of 40dB, and the maximum measured SNR at a frame rate of 30Hz and an oversampling ratio of 64 is approximately 43dB. The fixed pattern noise was calculated to be approximately 1% using measured results from the D/A converter and photodiode†. The static power dissipation of each $\Sigma\Delta$ ADC is less than 30nW (assuming a frame rate of 30Hz and an oversampling ratio of 64).

Figure 9 shows the measured MCBS ADC transfer functions for 16 different converters. The ADC measured integral and differential nonlinearities are 2.3 LSB and 1.2 LSB at 8 bits, respectively. The pixel gain and offset FPN due to ADC are 0.24% and 0.2% respectively. The static power dissipation of each pixel level MCBS ADC is less than 30nW (assuming 2.56ms conversion and 8 bit resolution).

*The ratio of the maximum shuttered non-saturating photocurrent to the dark current.

†This is a function of the minimum value of **STORE** as shown in equation 2.

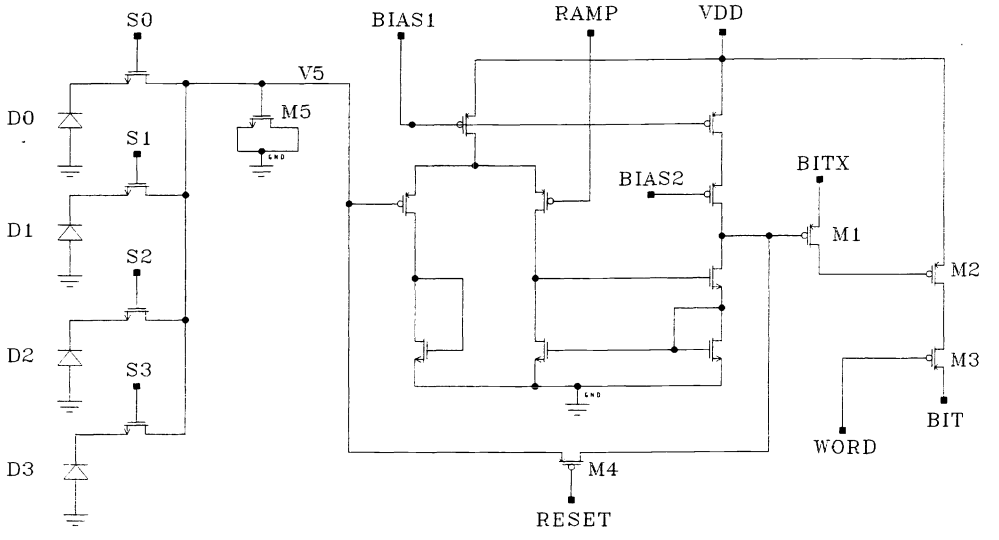

Figure 7. Four pixels sharing a MCBS ADC circuit.

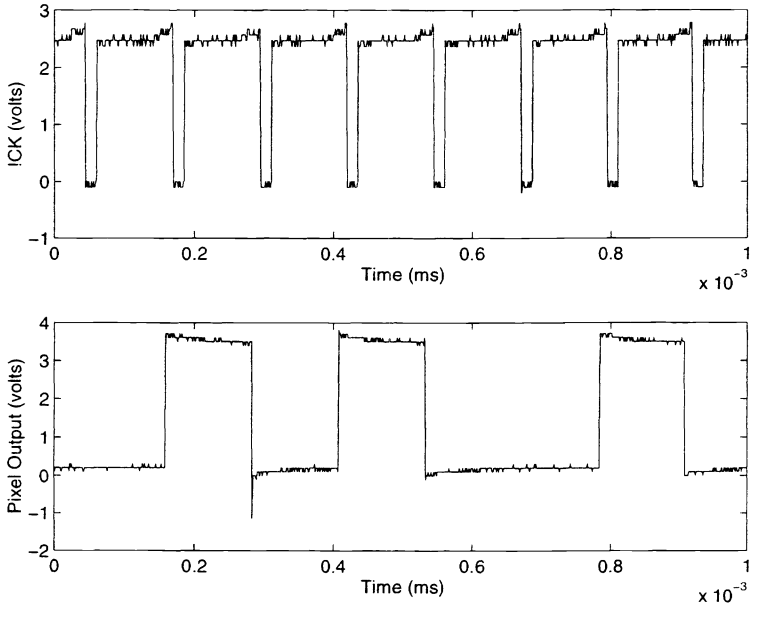

Figure 8. Single pixel $\Sigma\Delta$ ADC output from HP54601A. The top graph is **CK** bar and the bottom graph is the pixel output verses time.

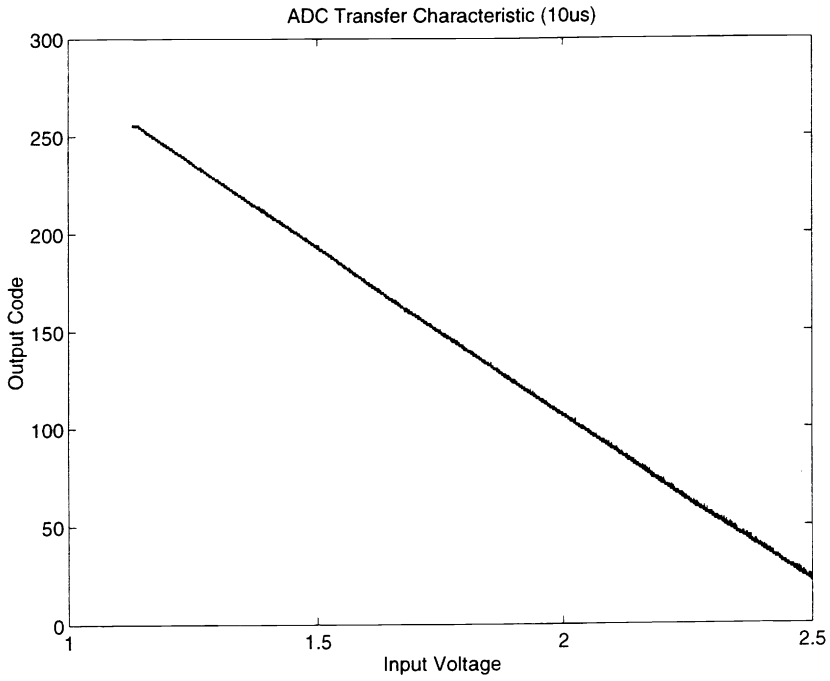

Figure 9. ADC transfer curve at 2.56ms conversion time (10μs per comparison)

	$\Sigma\Delta$ ADC	MCBS ADC
Technology	0.8 μm 3M1P	0.35μm 4M1P
Pixel Area	20.8 μm $\times$ 19.8 μm	8.9 μm $\times$ 8.9 μm
Transistors per pixel	4.25 (17 per four pixels)	4.5 (18 per four pixels)
Fill Factor	30%	25%
Array Size	128$\times$128	320$\times$240
Supply Voltage	3.3 v	3.3 v

Table 1. Process and Sensor Characteristics

5. COMPARISON

A direct comparison between ΣΔ ADC and MCBS ADC yields the following observations. The ΣΔ ADC and the MCBS ADC are about the same size, but the ΣΔ ADC has larger charge handling capacity than the MCBS ADC. The ΣΔ ADC has higher FPN than the MCBS ADC, but the ΣΔ ADC is more robust to transistor noise than the MCBS ADC. The output data rate of the ΣΔ ADC is larger than the MCBS ADC by the factor shown in equation 3. Quantization of the ΣΔ ADC is nonuniform and fixed by the desired oversampling ratio, while the MCBS ADC has programmable quantization intervals.[8] The ΣΔ ADC requires external processing to perform decimation of the data to the Nyquist frequency, and the MCBS ADC requires no external processing. The memory required to hold one frame of image data for the ΣΔ ADC is larger than the MCBS ADC by the factor shown in equation 3. Although the static power dissipation of both ADCs are about the same, the ΣΔ ADC generates more data and therefore, dissipates more dynamic power that the MCBS ADC. These comparisons are summarized in Table 5.

From this comparison we conclude that neither technique is clearly superior to the other. Depending on the application, e.g. visible or IR imagers, one technique may be better suited than the other. The pixel level ΣΔ ADC should be better suited to IR applications, which require large charge handling capability, and fine quantization near the middle of the input range, i.e. determining small differences between large charge values. In addition the moderate FPN associated with ΣΔ ADC causes very little degradation in system performance, since most IR sensors have large pixel FPN.

On the other hand, the MCBS ADC is well suited to visible applications where low FPN and low data rates are required. Voltage mode conversion also allows for high conversion gain from charge to voltage using small capacitors[‡]. Finally the control of **RAMP** and **BITX** allow quantization intervals to be arbitrarily adjusted for functions such as gamma correction.

	ΣΔ ADC	MCBS ADC
Size	4.25 transistors per pixel	4.5 transistor per pixel
Conversion mode	Charge to bits	Voltage to bits
Charge handling Capacity	Large	Small
FPN	Moderate	Small
Transistor noise sensitivity	Small	Moderate
Date rate	Large	Small
Quantization	Nonuniform - fixed by L	Programmable
External processing	Decimation Filtering	None
Required memory	Large	Small
Power Dissipation	Moderate	Small

Table 2. ADC Comparison

6. CONCLUSIONS

We presented two techniques for pixel level ADC, a ΣΔ modulation technique and the MCBS ADC. We compared the ADCs based on size, charge handling capacity, FPN, transistor noise sensitivity, data rate, quantization, power dissipation, and memory and external processing requirements. We concluded that the ΣΔ ADC is better suited to IR imaging, while the MCBS ADC is better suited to imaging in the visible range.

ACKNOWLEDGEMENTS

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[‡]This was not exploited in the implementation presented is this paper.

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