

A compact and lossless 8×8 SOA gate switch subsystem for WDM optical packet interconnections

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Abstract

We developed a compact 8×8 gate switch subsystem, which was integrated with eight 8:1 SOA modules (72-SOAs). We achieved a high-speed switching, lossless and colored operation.

Introduction

Large scalable and high-speed optical switches are necessary to achieve high bandwidth, low latency, and fine granularity for an ultra-high-performance computing (UHPC) system and an optical packet switching (OPS) system. We proposed a broadcast-and-select optical switch architecture with multi-gate SOAs (an MGSOA architecture), which have a fast switching characteristic on the nano-second order [1]. This architecture also achieves a high extinction ratio and suppresses neighbouring channel crosstalk because of unbiased SOA absorption. The MGSOA architecture can extend per-port base switch capacity by simultaneous switching of WDM packet signals. However, the number of SOA gate switches increases in proportion to the square number of ports. Therefore, we developed a monolithically-integrated SOA chip and a hermetically sealed module coupled with an array fiber on a Peltier cooler to maintain the reliability, scalability, and the switching speed [2, 3]. This module can also reduce the size, cost, and power consumption for a large port-count MGSOA architecture.

In this study, we developed, to our knowledge, the first compact 8×8 SOA gate switch subsystem. We present our evaluation of its characteristics, which demonstrate the feasibility of the MGSOA architecture.

Configuration of 8×8 SOA switch subsystem

The configuration of the 8×8 SOA gate switch subsystem with eight 8:1 SOA switch modules is shown in Fig. 1. First, the label signal (whose wavelength is 1310 nm) including destination information is sent to a packet scheduler through a WDM filter. Second, the subsystem controller selects the optical path corresponding to the destination port based on a command from the packet scheduler. The packet scheduler requires sending WDM packets to the transponder with adjusting skews between the label signal and the packet signals after sending a command to the subsystem. Finally, the packet signals multiplexing in the c-band are input to the subsystem, divided by a 1×8 splitter, and distributed to each SOA. The subsystem controller drives two

cascaded SOAs (SOA #9 and one of the arrays) simultaneously. The signal path is connected by an SOA in the ON state, and cross talk is suppressed by an SOA in the OFF state for a high optical signal-to-noise ratio (OSNR) and a high extinction ratio. It also achieves a lossless operation because of the gain of the SOA to compensate for the optical signal losses due to power splitting in the couplers.

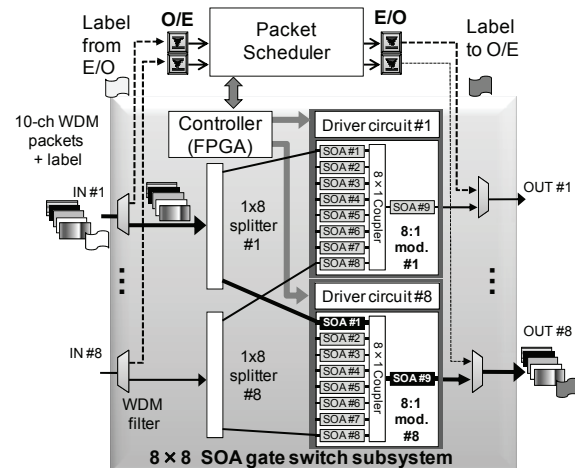


Figure 1: Configuration of 8×8 SOA gate switch subsystem using 8:1 SOA switch module

This subsystem has eight 8:1 SOA modules, and each SOA module has nine SOA elements. Therefore, the subsystem controls all of the 72 SOA drivers with all the signal and power lines wired by a delay line of equal length. Each SOA driver also requires a driving current of 300 mA in the ON state during an application of simultaneous switching WDM signals to avoid waveform degradation caused by the pattern effect. In addition, impedance matching that introduces a series resistance cannot be applied owing to large heat dissipation. Thus, we applied an equal-length wiring and a pre-emphasis of driving current using inductance to each SOA driver to satisfy high speed switching and high output current together [4]. We conducted a circuit simulation to evaluate the influences of the pre-emphasis technique on the switching speed using the length of delay line to each SOA chip. The results are shown in Table 1. Applying the pre-emphasis technique does not influence the

pattern length very much. Therefore, we designed a SOA driver circuit with an equal-length of less than 40 mm for each SOA chip for smart integration.

Pre-emphasis technique	Pattern length from SOA driver to SOA chip			unit
	20 mm	30 mm	40 mm	
OFF	3.3	5.0	6.5	ns
ON	1.7	2.2	2.5	

Table 1: Circuit simulation of rise time (Tr)

Subsystem characteristics

Fig. 2 shows a proto-type of an 8x8 SOA gate switch subsystem equipped with a control board, eight driver boards accommodating nine driver circuits, a TEC control circuit, and it shows an 8:1 SOA module, a 16-ch PD-array for monitoring input and output power, and a power supply in a 19-inch 2U-sized rack. The maximum power consumption is 143 W@100 VAC.

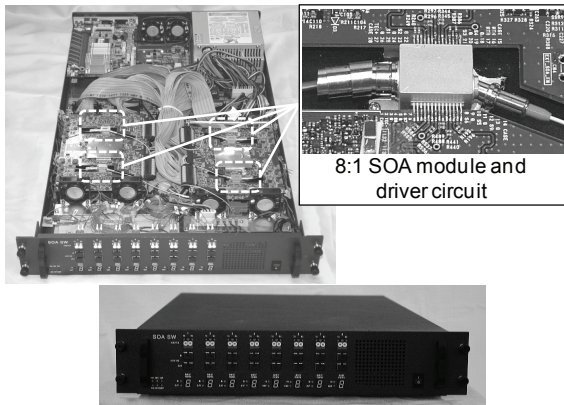


Figure 2: 8x8 SOA gate switch subsystem (19-inch 2U sized rack)

The continuous switching characteristics of an OPS primitive are shown in Fig. 3. The continuous wave (cw) light launched into IN#1 was switched periodically every 1.2 μs. The switching time of the rise time (Tr) and fall time (Tf) were achieved in 2.5 and 1.0 ns, respectively, for all ports.

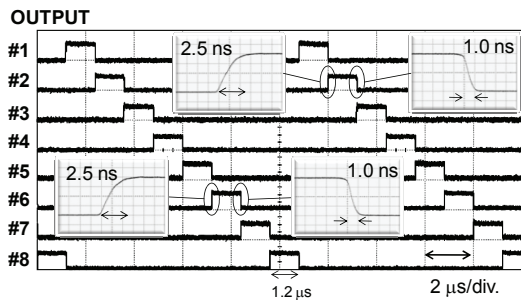


Figure 3: Switching characteristics

Next, we evaluated the bit-error rate (BER) characteristics of 10 Gbps NRZ, WDM packets. The input and output spectrum of 400 GHz spacing, 10-ch WDM signals are shown in Fig. 4. We suppressed four wave mixing (FWM) and maintained a fine OSNR of more than 29.4 dB, achieving a lossless operation of the total input and output power of +5 dBm (-5

dBm/ch) and +6 dBm (-4 dBm/ch). The payload pattern of the WDM packet signals is shown in Fig. 5. The lengths of the payload and guard time are 1,155 (1,443 byte@10G) and 45 ns (56 byte@10G), respectively. Fig. 6 shows the results of the OSNR and packet-triggered eye-diagrams compared to back to back at BER = 1x10⁻¹², where WDM packets launched into IN#5 and IN#7 were switched to OUT#7. We obtained a clear eye opening and a low power penalty of less than 1.0 dB for all wavelengths. Another port connection obtained almost the same results for OSNR penalty: less than 1.0 dB.

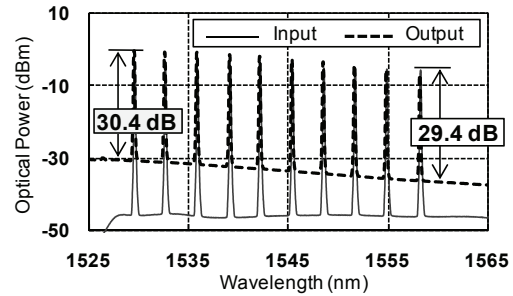


Figure 4: Output spectrum of 10-ch WDM signal

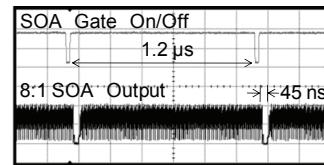


Figure 5: Payload pattern of 10-ch WDM packets

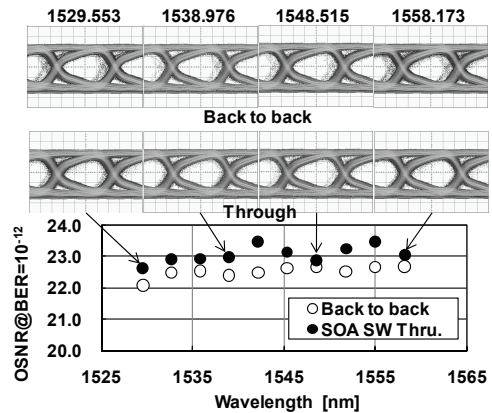


Figure 6: Power penalty and triggered eye-diagrams

Conclusions

We described a compact 8 x 8 SOA gate switch subsystem and demonstrated the feasibility of its high-speed WDM packet switching and transmission characteristics with lossless and low power penalty.

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References

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